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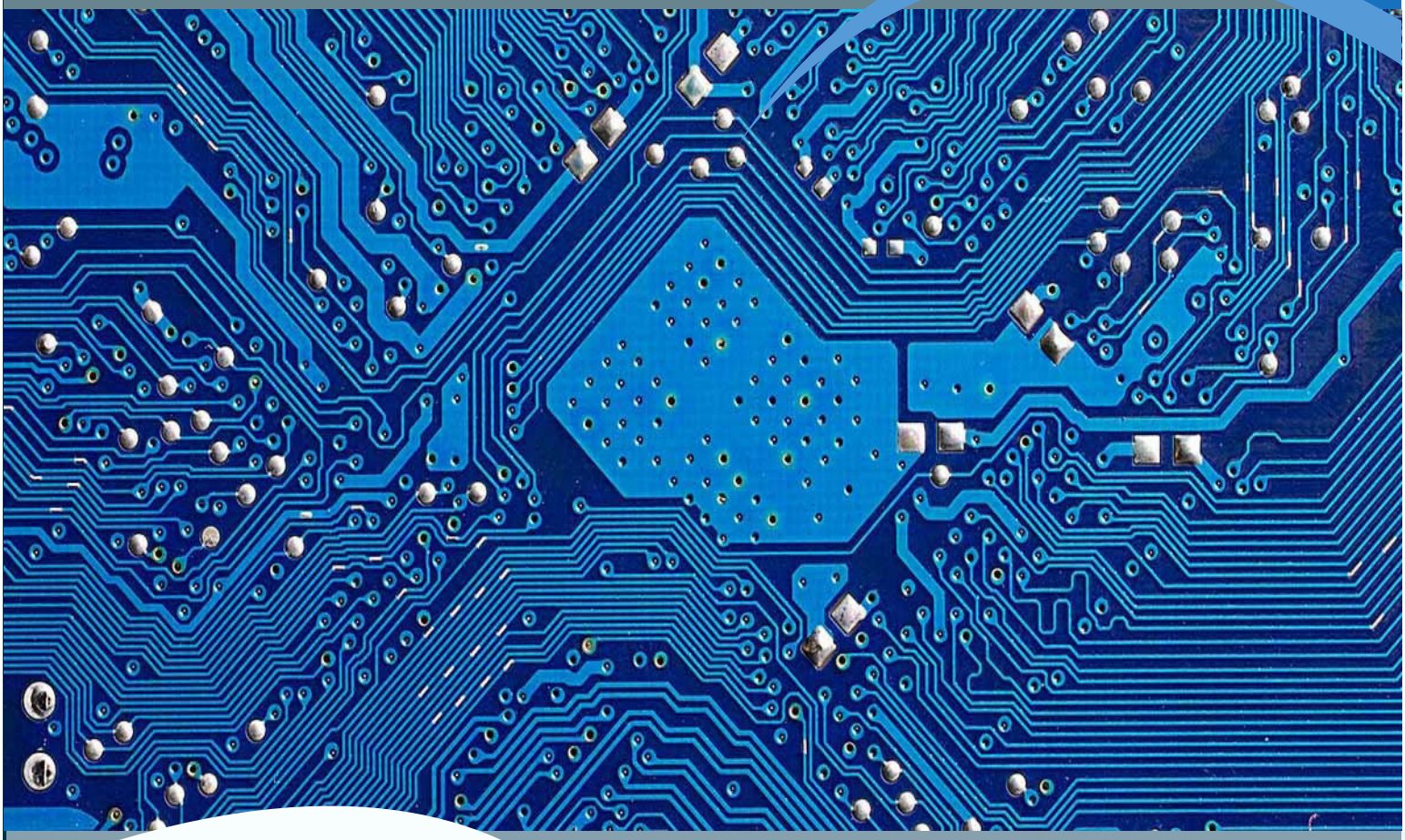

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Editorial

In the era of telephones very few had predicted its wide impact on mankind. Initially from the bulky telephone sets gradually moving on towards smaller and more sophisticated handy versions, the telecommunication system has come a long way. The birth of cellular phones, popularly referred to as cell phones or mobile phones created endless possibilities in the field of communication. The cell phones which were used till the early 90's were mere wireless hand set phones for verbal communications. But in the late 90's and during the dawn of 21st.century brought the paradigm to a new level. The cell phones were now developed not only for the purpose of making calls but also for a range of other purposes. The term 'Smartphone' came into existence in true sense only after the launch of the revolutionary product form Apple, called the 'iPhone'(2007) which changed the way people looked at mobile phone. It is no longer a medium for communication rather an important part of life and the Smartphone market has never again looked back ever since. In just 5 years the Smartphone became, from a mere Electronics device to a bare necessity.

The Smartphones today already possess a wide range of features ranging from providing high internet access to health monitoring. They have now become a one stop solution for all problems. Today the controller of an organization can keep a track of what is happening in his office even, he is miles away. Even a layman can easily learn to operate the smartphones in a few hours as it is very user-friendly. Now this tremendous improvement is something that has taken place in a time span of 5 years. Imagine what would happen in another say 5 years, or 10 years, or say 100 years? Where will this technology drive the mankind to? In the future, they may evolve into personal mobile computers. Assuming that Moore's law holds true, mobile CPUs with near supercomputing speeds will be entirely possible. The number, accuracy and performance of sensors will grow, the combination of which will give the users a very powerful sense of the surroundings.

It might even take place of a wrist watch which would make use of peripherals, like information glasses and headsets, not only these peripherals allow the user to explicitly interact with the digital and physical word, but they'll also provide subtle cues to users subconscious. As a developer, engineer and product designer one might be working on something beyond expectations. Who knows, what the future will give the society but one can at least be sure of one thing, that is, the current technologies will shape the future. Therefore it is rightly said

"Inventor: A person who makes an ingenious arrangement

of wheels, levers and springs, and believes it's civilization." *Ambrose Bierce*

So this conference has been designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these disciplines of engineering. It is pleasure to welcome all the participants, delegates and organizer to this international conference on behalf IOAJ family members. IOAJ has received a great response from all parts of country and abroad for the presentation and publication in the proceeding of the conference.

I sincerely thank all the authors for their valuable contribution to this conference. I am indebted towards the reviewers and Board of Editors for their generous gifts of time, energy and effort.

Editor-in-Chief

Dr. Srikanta Patnaik

A HIGH PERFORMANCE PARALLEL DISTRIBUTED ARITHMETIC DCT ARCHITECTURE

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Abstract— In this brief, by operating the shifting and addition in parallel, an error-compensated adder-tree (ECAT) is proposed to deal with the truncation errors and to achieve low-error and high-throughput discrete cosine transform (DCT) design. Instead of the 12 bits used in previous works, 9-bit distributed arithmetic-precision is chosen for this work so as to meet peak-signal-to-noise-ratio (PSNR) requirements. Thus, an area-ef-ficient DCT core is implemented to achieve 1 Gpels/s throughput rate with gate counts of 22.2 K for the PSNR requirements outlined in the previous works.

Keywords -Distributed arithmetic (DA)-based, error-compensated adder-tree (ECAT), 2-D discrete cosine transform (DCT).

I. INTRODUCTION

Discrete cosine transform (DCT) is a widely used tool in image and video compression applications. Recently, the high-throughput DCT designs have been adopted to fit the requirements of real-time applications.

To reduce area, ROM-based distributed arithmetic (DA) was applied in DCTcores .Uramoto*etal* implemented the DA-based multipliers using ROMs to produce partial products together with adders that accumulated these partial products. In this way, instead of multipliers, the DA-based ROM can be applied in a DCT core design to reduce the area required. In addition, the symmetrical properties of the DCT transform and parallel DA architecture can be used in reducing the ROM size. Shams *et al.* employed a bit-level sharing scheme to construct the adder-based butterfly matrix called new DA (NEDA)]. Being compressed, the butterfly-adder-matrix in utilized 35 adders and 8 shift-addition elements to replace the ROM. Based on NEDA architecture, the recursive form and arithmetic logic unit (ALU) were applied in DCT design to reduce area cost. Hence the NEDA architecture is the smallest architecture for DA-based DCT core designs, but speed limitations exist in the operations of serial shifting and addition after the DA-computation. The high-throughput shift-adder-tree (SAT) and adder-tree (AT), those unroll the number of shifting and addition words in parallel for DA-based computation. However, a large truncation error occurred. In order to reduce the truncation error effect, several error compensation bias methods have been presented based on statistical analysis of the relationship between partial products and multiplier-multiplicand. However, the elements of the truncation part outlined in this work are independent so that the previously described compensation methods cannot be applied.

This brief addresses a DA-based DCT core with an error-compensated adder-tree (ECAT). The proposed ECAT operates shifting and addition in parallel by unrolling all the words required to be computed. Furthermore, the error-compensated circuit alleviates the truncation error for high accuracy design. Based on low-error ECAT, the DA-precision in this work is chosen to be 9 bits instead of the traditional 12 bits so as to achieve the peak-signal-to-noise-ratio (PSNR) requirements. Therefore, the hardware cost is reduced, and the speed is improved using the proposed ECAT.

This brief is organized as follows. In Section II, the mathematical derivation of the distributed arithmetic is given. The proposed ECAT architecture is discussed in Section III. The proposed 8 8 2-D DCT core is demonstrated in Section IV. The comparisons and results are presented in Section V, and conclusions are drawn in Section VI.

II. MATHEMATIAL DERIVATION OF DISTRIBUTED ARITHMETIC

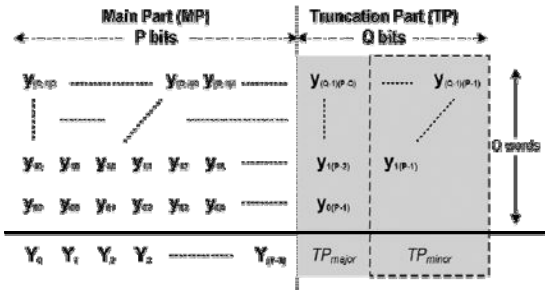
The inner product is an important tool in digital signal processing applications. It can be written as follows:

$$Y = A^T X = \sum_{i=1}^{L} A_i X_i \qquad (1)$$

Whee Ai, Xi, and L are with fixed coefficient, with input data, and number of inputs, respectively. Assume that coefficient A_i is Q-bit two's complement binary fraction number. Equation (1) can be expressed as follows:

$$Y = \begin{bmatrix} 2^{0} & 2^{-1} & \cdots & 2^{-(Q-1)} \end{bmatrix} \begin{bmatrix} A_{1,0} & A_{2,0} & \cdots & A_{L,0} \\ A_{1,1} & A_{2,1} & \cdots & A_{L,1} \\ \vdots & \vdots & \ddots & \vdots \\ A_{1,(Q-1)} & A_{2,(Q-1)} & \cdots & A_{L,(Q-1)} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_L \end{bmatrix}$$

$$= \begin{bmatrix} 2^{n} & 2^{-1} & \cdots & 2^{-(Q-1)} \end{bmatrix} \begin{bmatrix} y_0 \\ y_1 \\ \vdots \\ y_{(Q-1)} \end{bmatrix} \quad (2)$$



Where $y_j = \sum_{i=1}^{L} A_{i,j} X_i, A_{i,j} \in \{0,1\}$ for $1 \le j \le (Q-1)$, and $A_{i,j} \in \{-1, 0\}$ for $j = 0$, Note that y_0 may be 0 or a negative number due to two's complement representation. In (2), y_j values. Thus the inner product computation in (1) can Fig.1. Q-P-bit words shifting and addition operations is parallel. be implemented by using shifting and adders instead of multipliers. Therefore, low hardware cost can be achieved by sing DA-based architecture.

III. ECAT ARCHITECTURE

From (2), the shifting and addition computation can be written as follows :

$$Y = \sum_{j=0}^{Q-1} y_j, 2^{-1} \quad (3)$$

In general, the shifting and addition computation uses a shift-and-add operator in VLSI implementation in order to reduce hardware cost. However, when the number of the shifting and addition words increases, the computation time will also increase. Therefore, the shift-adder-tree (SAT) presented in operates shifting and addition in parallel by unrolling all the words needed to be computed for high-speed applications. However, a large truncation error occurs in SAT, and an ECAT architecture is proposed in this brief to compensate for the truncation error in high-speed applications.

In Fig. 1, the Q P-bit words operate the shifting and addition in parallel by unrolling all computations. Furthermore, the operation in Fig. 1 can be divided into two parts: the main part (MP) that includes most significant bits (MSBs) and the truncation part (TP) that has least significant bits (LSBs). Then, the shifting and addition output can be expressed as follows:

$$Y = \mathrm{M\,P} + \mathrm{T\,P}2^{-(P-2)} \quad (4)$$

The output Y will obtain the P-bit MSBs using a rounding operation called post truncation (Post-T), which is used for high-accuracy applications. However, hardware cost increases in the VLSI design. In general, the TP is usually truncated to reduce hardware costs in parallel shifting and addition operations, known as the direct truncation (Direct-T) method. Thus, a large truncation error occurs due to the neglecting of carry propagation from the TP to MP. In order to alleviate the truncation error effect, several error compensation bias methods have been presented]. All previous works were only applied in the design of a fixed-width multiplier. Because the products in a multiplier have a relationship between the input multiplier and multiplicand, the compensation methods usually use the correlation of inputs to calculate a fixed or an adaptive compensation bias using simulation or statistical analysis. Note that the addition elements in the TP in Fig. 1 (where $1 \le q \le (Q-1)$ and $(P-q-1) \le p \le (P-1)$ are independent from each other. Therefore, the previous compensation method cannot be applied in this work, and the proposed ECAT is explained as follows.

A. Proposed Error-Compensated Scheme

From Fig.1, (4) can be approximated as

$$Y \approx \mathrm{MP} + \sigma \cdot 2^{-(P-2)} \quad (5)$$

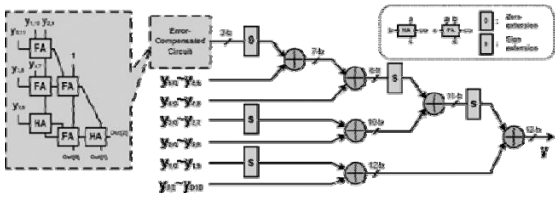


Fig.2 Proposed ECAT architecutre of shifting and addition operators for the (*P*, *Q*) = (1, 26) example.

Where σ is the compensated bias from the TP to the MP as listed in (6)–(8)

$$\sigma = \mathrm{Round}\left(\mathrm{TP}_{\mathrm{major}} + \mathrm{T\,P}_{\mathrm{minor}}\right) \quad (6)$$

and

$$\mathrm{TP}_{\mathrm{minor}} = \frac{1}{2}\sum_{j=0}^{Q-1} y_{j(P-1-j)} \quad (7)$$

$$\mathrm{TP}_{\mathrm{minor}} = \frac{1}{4}\left(y_{1(P-1)+\ldots+y(Q-1)(P-Q+1)}\right) + \frac{1}{8}\left(y_{2(P-1)+\ldots+y(Q-1)(P-Q+2)}\right) + \left(\frac{1}{2}\right)^{Q} y_{(Q-1)(P-1)} \quad (8)$$

Where Round() is rounded to the nearest inter. The $\mathrm{TP}_{\mathrm{major}}$ has more weight than $\mathrm{TP}_{\mathrm{minor}}$ when contributing towards the σ. Therefore, the

compensated bias σ can be calculated by obtaining TP_{major} and estimating TP_{minor}. Let the probability of $y_{qp} = 1$ be 0.5, where $1 \le q \le (Q - 1)$ and $(P - q - 1) \le (P - 1)$. Hence, (8) can be expressed as follows:

$$TP_{minor} = \frac{1}{4}\left(\frac{1}{2}(Q-1)\right) + \ldots + \left(\frac{1}{2}\right)^{Q+1} = \left(\frac{1}{2}\right)^{Q+2} \sum_{n=1}^{Q-1} n.2^{n} = \frac{(Q-2)}{4} + \left(\frac{1}{2}\right)^{Q+1} \quad (9)$$

For a given TP_{major}, $\left(y_{j(p-1-j)},\ 0 \le j \le (Q-1)\right)$, the σ can be obtained after rounding the sum of $\left(TP_{major} + TP_{minor}\right)$. In order to round the summation, TP_{minor} can be divided into four parts:

$$TP_{minor} = \begin{cases} k - \frac{1}{2} + \left(\frac{1}{2}\right)^{4k+1}, & \text{for } Q = 4k \\ k - \frac{1}{4} + \left(\frac{1}{2}\right)^{4k+2}, & \text{for } Q = 4k+1 \\ k + \left(\frac{1}{2}\right)^{4k+3}, & \text{for } Q = 4k+2 \\ k + \frac{1}{4} + \left(\frac{1}{2}\right)^{4k+4}, & \text{for } Q = 4k+3. \end{cases} \quad (10)$$

As $k \ge 1$, the TP_{minor} approximates (11)

$$TP_{minor} \approx \begin{cases} (k-1) + \frac{1}{2}, & \text{for } Q = 4k \\ (k-1) + \frac{3}{4}, & \text{for } Q = 4k+1 \\ k, & \text{for } Q = 4k+2 \\ k + \frac{1}{4}, & \text{for } Q = 4k+3. \end{cases} \quad (11)$$

Hence, σ can be rewritten as three cases.

Case 1) $Q = 0, 1, 2, 3$

$$\sigma = \text{Round}\left(TP_{major}\right),$$

Case 2) $Q = 4k, 4k+1 (k \ge 1)$

$$\sigma = (k-1) + \text{Round}\left(TP_{major} + 0.5\right), \quad (13)$$

TABLE I
COMPARISONS OF ABSOLUTE AVERAGE ERROR ∈, MAXIMUM

Error	(P, Q)	(12, 3) case1	(12, 6) case3	(12, 9) case2	(12, 12)
ε	Direct-T	1.0625	2.5078	4.0010	5.5001
	Proposed	0.2656	0.3789	0.3804	0.4738
	Post-T	0.2500	0.2500	0.2500	0.2500
ε_{max}	Direct-T	2.1250	5.0156	8.0020	11.000
	Proposed	0.6250	1.5000	2.0020	3.0000
	Post-T	0.5000	0.5000	0.5000	0.5000
ε	Direct-T	1.3516	6.7614	16.730	31.224
	Proposed	0.1016	0.2184	0.2222	0.3472
	Post-T	0.0859	0.0834	0.0833	0.0833

Case 3) $Q = 4k+2, 4k+3 (k \ge 1)$

$$\sigma = k + \text{Round}\left(TP_{major}\right), \quad (14)$$

B. Performance Simulation for an Error-Compensated Circuit

In this subsection, comparisons of the absolute average error ε, the maximum error $\in_{max}$, and the mean square error $\in_{max}$, for the proposed error=compensated circuit with Direct-T and Post-T are listed in Table I.

The ε, $\in_{max}$, and $\in_{max}$, are defined as follows:

$$\in = Avg\left[\left|TP - \sigma\right|\right] \quad (15)$$

$$\varepsilon_{max} = \max\left\{\left|TP = \sigma\right|\right\} \quad (16)$$

$$\varepsilon_{max} = Avg\left\{\left(TP = \sigma\right)^2\right\} \quad (17)$$

Where $Avg\{\}$ is the average operator.

The internal word-length usually uses 12 bits in a DCT design. Consequently, word length P = 12 is chosen together with different values of 3, 6, 9, and 12, which are listed in Table I. The Post-T method provides the most accurate values for fixed-width computation nowadays. In addition, the Direct-T method has the largest inaccuracies of the errors shown in Table I for low-cost hardware design. The proposed ECAT is more accurate than Direct-T and is close to the performance of the Post-T method using a compensated circuit. Because the truncation part TP_{minor} is estimated using statistical analysis, the magnitude of errors also increases as the number of shift-and-add words *Q* increases.

C. Proposed ECAT Architecture

The proposed ECAT architecture is illustrated in Fig. 2 for (*P, Q*) = (12,6) ((*case 3*), where block FA indicates a full-adder cell with three inputs (a, b, and c) and two outputs, a sum (s) and a carry-out (co). Also, block HA indicates half-

TABLE II
COMPARISONS OF ABSOLUTE AVERAGE ERROR ∈, MAXIMUM ABSOLUTE ERROR $\in_{max}$, AND MEAN SQUARE ERROR $\in_{mse}$

	Shift-and-add	SAT	Proposed ECAT
Area (gates)	236	406	463
Delay (ns)	10.8	3.72	3.89
Area × delay	100 %	59.3 %	70.7 %
$\in_{mse}$	0.326	6.761	0.218

adder cell with two inputs (a and b) and two outputs, a sum (s) and a carry-out(co). The comparisons of area, delay, area-delay product, and accuracy for the proposed ECAT with other architectures are listed in Table II. The area and delay are synthesized using a Synopsys Design Compiler with the Artisan TSMC 0.18- μm Standard cell library.

The proposed ECAT has the highest accuracy with a moderate area-delay product. The shift-and-add method has the smallest area, but the overall computation time is equal to $10.8(=1.8\times 6)$ ns that is the longest. Similarly, the SAT, which truncates the TP and computes in parallel, takes 3.72 ns to complete the computation and uses 406 gates, which is the best area-delay product performance. However, for system accuracy, the SAT is the worst option shown in Table II. Therefore, the ECAT is suitable for high-speed and low-error applications.

IV. PROPOSED 8 2 D DCT CORE DESIGN

The 1-D DCT employs the DA-based architecture and the proposed ECAT to achieve a high-speed, small area, and low- error design. The 1-D 8-point DCT can be expressed as follows:

$$Z_n \frac{1}{2} k_n \sum_{m=0}^{7} x_m \times \cos\left(\frac{(2m+1)n\pi}{16}\right) \qquad (18)$$

Where x_m denotes the input data; Z_n denotes the transform output; $0 \le n \le 7; k_n = 1/\sqrt{2}$ for $n = 0$; and $k_n = 1$ for other n values. By neglecting the scaling factor 1/2, the 1-D 8-point DCT in (18 can be divided into even and odd parts: $\mathbf{Z}_e$ and $\mathbf{Z}_o$ as listed in (19) and (20), respectively.

$$\mathbf{Z}_e = \begin{bmatrix} Z_0 \\ Z_2 \\ Z_4 \\ Z_6 \end{bmatrix} = \begin{bmatrix} c_4 & c_4 & c_4 & c_4 \\ c_2 & c_6 & -c_6 & -c_2 \\ c_4 & -c_4 & -c_4 & c_4 \\ c_6 & -c_2 & c_2 & -c_6 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_3 \end{bmatrix} = \mathbf{C}_e \cdot \mathbf{a} \quad (19$$

$$\mathbf{Z}_o = \begin{bmatrix} Z_1 \\ Z_3 \\ Z_5 \\ Z_7 \end{bmatrix} = \begin{bmatrix} c_1 & c_3 & c_5 & c_7 \\ c_3 & -c_7 & -c_1 & -c_5 \\ c_5 & -c_1 & c_7 & c_3 \\ c_7 & -c_5 & c_3 & -c_1 \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix} = \mathbf{C}_e \cdot \mathbf{b} \quad (20$$

Where $c_i = \cos(i\pi/16)$. Moreover, the even part $\mathbf{Z}_e$ can be further decomposed into even and odd parts: $\mathbf{Z}_{ee}$ and $\mathbf{Z}_{eo}$

$$\mathbf{Z}_{ee} = \begin{bmatrix} Z_0 \\ Z_4 \end{bmatrix} = \begin{bmatrix} c_4 & c_4 \\ c_4 & -c_4 \end{bmatrix} \begin{bmatrix} A_0 \\ A_1 \end{bmatrix} = \mathbf{C}_{ee} \cdot \mathbf{A} \quad (21$$

$$\mathbf{Z}_{eo} = \begin{bmatrix} Z_2 \\ Z_6 \end{bmatrix} = \begin{bmatrix} c_2 & c_6 \\ c_6 & -c_2 \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \end{bmatrix} = \mathbf{C}_{eo} \cdot \mathbf{B} \quad (22$$

For the DA-based computation, the coefficient matrix $\mathbf{C}_o$, $\mathbf{C}_{ee}$, and $\mathbf{C}_{e0}$, are expressed as 9-bit binary fraction numbers. Table III expresses $\mathbf{Z}_{ee}$ (Z_0 and Z_4) in the bit level formulation. In Table III, using given input data A_0 and A_1, the

TABLE III
9-BIT DA-BASED COEFFICIENT MATRIX $\mathbf{C}_{ee}$

Z_0		Z_4	
Weight	Value	Weight	Value
-2^0	0	-2^0	A_1
2^{-1}	$A_0 + A_1$	2^{-1}	A_0
2^{-2}	0	2^{-2}	A_1
2^{-3}	$A_0 + A_1$	2^{-3}	A_0
2^{-4}	$A_0 + A_1$	2^{-4}	A_0
2^{-5}	0	2^{-5}	A_1
2^{-6}	$A_0 + A_1$	2^{-6}	A_0
2^{-7}	0	2^{-7}	A_1
2^{-8}	$A_0 + A_1$	2^{-8}	$A_0 + A_1$

transform output $\mathbf{Z}_{ee}$ needs only one adder to compute ($A_0 + A_1$) and two separated ECATs to obtain the results of Z_0 and Z_4. Similarly, the other transform outputs $\mathbf{Z}_{eo}$ and $\mathbf{Z}_o$ can be implemented in DA-based forms using 10(= 1 + 9)

adders and corresponding ECATs. Consequently, from the (19)–(22), the proposed 1-D 8-point DCT architecture can be constructed as illustrated in Fig. 3 using a DA-Butterfly-Matrix, that includes two DA even processing elements (DAEs), a DA odd processing element (DAO) and 12 adders/subtractors, and 8 ECATs (one ECAT for each transform output). The eight separated ECATs work simultaneously, enabling high-speed applications to be achieved. After the data output from the DA-Butterfly-Matrix is completed, the transform output $\mathbf{Z}$ will be completed during one clock cycle by the proposed ECATs. In contrast, the traditional shift-and-add architecture requires Q clock cycles to complete the transform $\mathbf{Z}$ output if the DA-precision is Q bits.

With high-speed considerations in mind, the proposed 2-D DCT is designed using two 1-D DCT cores and one transpose buffer. For accuracy, the DA-precision and transpose buffer word lengths are chosen to be 9 bits and 12 bits, respectively, meaning that the system can meet the PSNR requirements

outlined in previous works. Moreover, the 2-D DCT core accepts 9-bit image input and 12-bit output precision.

For the proposed 2-D DCT, the Synopsys Design Compiler was applied to synthesize the RTL design of the proposed core, and the Cadence SoC Encounter was adopted for placement and routing (P&R). Implemented in a 1.8-V TSMC 0.18-µm 1P6M CMOS process, the proposed 8 × 8 2-D DCT core has a latency of 10 clock cycles and is operated at 125 MHz. As a result of the 8 parallel outputs, the proposed 2-D DCT core can achieve a throughput rate of 1 Gpixels per second (= 8 × 125 MHz), meeting the 1080 p (1920 × 1080 × 60 pixels/s) high definition television (HDTV) specifications for 200 MHz based on low power operations. The core layout and simulated characteristics are shown in Fig. 4.

Table IV compares the proposed 8 × 8 2-D DCT core with previous 2-D DCT cores. In [3], a multiplier-based DCT core based on pipeline radix-42 single delay feedback path (R42 SDF) architecture to achieve high-speed design. The ROM-based DCT core is presented to reduce hardware cost. A NEDA architecture is presented by using adders to reduce the chip area of DCT core. Nevertheless, a speed limitation for shift-and-add is in NEDA design. The SAT and AT architectures for DA-based DCTs improve the throughput rate of the NEDA method. However, DA-precision must be chosen as 13 bits to meet the system.

	Line et al. [3]	Uramoto et al.[4]	Shame et al. [7]	Chunagam et al. [10]	Huang et al. [11]	Proposed
Architecture	Multiplier-based	ROM-based	NEDA	DA-based	DA-based	DA-based
Technology	0.15µmm	0.8µm	0.18µm	0.18µm	0.18µm	0.18µm
Multipliers/ROMs	1.0	0.256	0.0	0.0	0.0	0.0
Adders	26	16	92	12+18ALU*+16SAT	50+16AT	46+16 ECAT
DA-precision	-	-	12 bits	13 bits	13 bits	9 bits
Throughput Rate (pels/sec)	100 M	100 M	77 M	250 M	400 M	1 G
Gate Counts (NAND2)	60 K	25.5 K	22.5 K	27.8 K	39.8 K	22.2 K
Hardware Efficiency	1.6	3.92	3.42	9	10.05	45
Accuracy (CCITT Compatible)	Yes	Yes	Yes	N/A	N/A	Yes

* ALU: Arithmetic logic unit. 4 transistors per NAND2 gate for different technology. CCITT: Consultative Committee for International Telegraph and Telephone.

★ ECAT: The proposed error-compensated adder-tree. 77 MHz 1 GHz , where denominator 13 is the number of shifting and addition computation cycles.

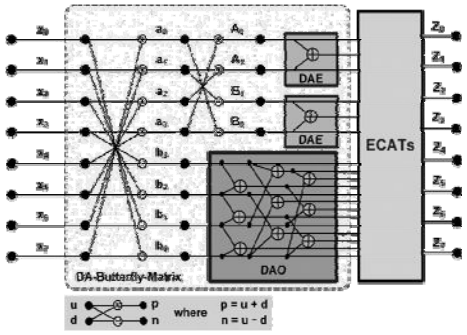


Fig. 3. Architecture of the proposed 1-D 8-point DCT

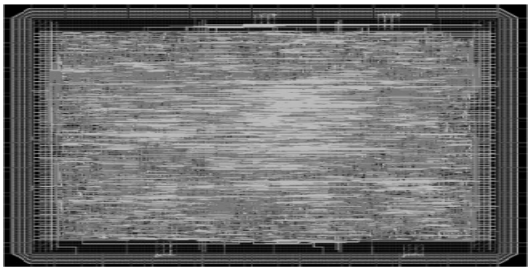


Fig.4. Core layout and characteristics

accuracy with more area overhead. The proposed DCT core uses low-error ECAT to achieve a high-speed design, and the DA-precision can be chosen as 9 bits to meet the PSNR requirements for reducing hardware costs. The proposed DCT core has the highest hardware efficiency, defined as follows (based on the accuracy required by the presented standards)

$$\text{Hardware Efficiency}(10^3 \text{ pels/s}) = \frac{\text{Throughput Rate}}{\text{Gate Counts}}. \quad (23)$$

TABLE III
9-BIT DA-BASED COEFFICIENT MATRIX ee C

FPGA-Chip	XC2VP30			XC3S200	
Architecture	[15]	[16]	Proposed	[17]	Proposed
# of 4 input LUTs	10310	2618	2990	2271	2847
# of Slices	5729	2823	1872	1221	1585
# of Slices Flip Flops	3736	3431	1837	616	1817
Clock Freq. (MHz)	149	107	99	50	61
Throughput (M-pels/s)	149	107	792	400	488
Power (mW)	N/A	N/A	166.8	281	91

Furthermore, the proposed 2-D DCT core synthesized by using Xilinx ISE 9.1, and the Xilinx XC2VP30 FPGA can achieve 792 mega pixels per second (M-pels/sec) throughput rate (up to about 7 folds of previous work . Table V compares the proposed 2-D DCT core with previous FPGA implementations.

CONCLUSION

In this brief, a high-speed and low-error 8 8 2-D DCT design with ECAT is proposed to improve the throughput rate significantly up to about 13 folds at high compression rates by operating the shifting and addition in parallel. Furthermore, the proposed error-compensated circuit alleviates the truncation error in ECAT. In this way, the DA-precision can be chosen as 9 bits instead of 12 bits so as to meet the PSNR requirements. Thus, the proposed DCT core has the highest hardware ef-ficiency than those in previous works for the same PSNR requirements. Finally, an area-efficient 2-D DCT core is implemented using a TSMC 0.18-μ m process, and the maximum throughput rate is 1 Gpels/s. In summary, the proposed architecture is suitable for high compression rate applications in VLSI designs.

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GAIT RECOGNITION USING ANGLE AND FUZZY LOGIC

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Abstract—this paper introducesa new gait recognition approach using angle computation and fuzzy logic. We proposed a gait system with the help of fuzzy inference system (FIS) for better gait recognition rate. This approach is tested on a databaseof video sequences, corresponding 17 people. The previous approaches of gait recognition are compared with our proposed method. We get better recognition rate as compared to previous methods. Our method is based on dynamic body parameters. We have taken two component of human body. The first component is hand and second component is feet. The second component is subdivided into two parts i.e. toe and heel of both right and left leg. Our proposed method increase the matching accuracy which is lies between 75 to 86 percent.

Keywords- Gait recognition, angle, fuzzylogic, FIS(fuzzy inference system),biometric.

I. INTRODUCTION

In the present world scenario, the importance of application requiring human identification, security measures has increased drastically and is ever growing. In response to this demand new technologies are being developed to achieve requisite level of security. One of these technologies is referred to as biometrics .biometrics refers to the automatic recognition of a person based on their physiological or behavioral characteristics. Physical and behavioral characteristics of each and every people are different and non transferable Human gait is an important and promising biometric resource for identification. Gait recognition is classified in to two methods namely model based and model free. In this paper we use Fuzzy inference system to achieve better gait recognition rate.

A new application of computer vision dealing with the analysis of images involving humans. There has been keen interest in human movement from a wide variety of disciplines [3].A literature including medical and physiological studies, indicating the potential of gait in personal identification, in psychology, a vast studies on human perception byJohansson[2].each biometrics has its pros and cons, and the choice depends on the application. No single biometric is expected to effectively meet the aspects of all the application. a specific biometric is choose for an application by matching the properties of biometric and the operational mode of the application.[1][12]. Biometric system is basically a pattern recognition system that operates by a collecting data from an individual, extracting a feature set from the collected data, and comparing this feature set against the template set in the database. Biometricsare face, fingerprint, DNA, iris and retinal patterns, voice, hand geometry, gait, ear and signature.Gait is the best biometric for human recognition. We create gait recognition system with the help of fuzzy inference system in our proposed method.

This paper is organized as follows. Section II Summaries some related existing methods for human gait recognition. Gait, fuzzylogic, fuzzy inference system and its methods and functions is described in section III.Section IV provides our proposed method.Experimental results & analysis are presented in section V, followed by Conclusions & future scope in Section VI.

II. RELATED WORK

A survey of the current analysis of human movement has been outlined by Gavrilla[3]. he surveyed the work on visual analysis looking at gestures and whole body movement and outlined ability to recognize people and their activities by computer. According to Garvilla[3] survey the visual analysis of human movement has become a major application in world of computer vision. An effective gait recognition approach based GEI (gait Energy image)was proposed by [X.Yang,Y.Zhang,T.Zhang, E.Gheng&J.Yang[5]]

Existing methods for gait recognition can be classified in two categories first is model based and 2nd is motionbased. Among the motion based ones, there is an effective method using Gait energy image as gait representation.GEI is the average silhouette over one gait cycle.

Human gait is a promising biometrics resource.[Xuelong Li. Stephen J .Maybank, Shuicheng Yan, Dacheng Tao, Dong Xu [7]] had studied gait components and their application to gender recognition. In their research, the information about gait was obtained from the motions of different parts of the silhouette. human silhouette was segmented in to seven components namely head ,arm,trunk,thigh, front leg , back leg and feet .this paper helped me a lot to write this paper , In my paper I have considered only five parts of the body namely hand , right heel, right toe, left heel and left toe .

[Joao P .Ferreira , Manuel Crisostomo, A. Paulo Coimbra, David Carnide , Antonio Marto [8]] did the

tracking and analysis of the human motion, specially the Gait, by using computational vision there's aim to obtain gait signatures using computer vision techniques and to extract kinematics features for describing motion of human, to obtain this , white LED placed on several points on an individual's body partsand guided by automatic knowledge ,gait properties were extracted.

This study goes some way towards the research work done by different researchers in the field of biometric resource gait. I have gone through the research work of different researchers that are dealt in study of gait.

III. GAIT AND FUZZY LOGIC

The definition of Gait is defined as "*A peculiar way or manner one walks*" and is a complex spatiotemporal biometrics. The walking style of every person is unique. Due to this it is sufficiently used for verification in security applications. Using gait as a biometric is a relatively new area of study .In computer vision recognizing humans by gait has recently been investigated. Human gait may be defined as a means of identifying individuals by the way they walk [10]

When we compared gait to other biometrics, gait has some unique characteristics. The most attractive feature of gait as a biometrics is its unobtrusiveness. It means, unlike other biometrics, it can be captured at a distance without physical contacts of the observed subject. Most other biometrics such as fingerprints, hand geometry, voice, face and signature can be captured only by physical contact or at a close distance from the recording instrument. Gait also has the advantage of being difficult to steal, hide or fake [13]

There are some limitations in gait capturing that make it difficult to identify and record all parameters that affect gait .it is affected by clothes, footwear, walking speed, and emotional condition etc.

Fuzzy logic is a mathematical approach to solving problems. It excels in producing exact result from imprecise data and is especially useful in computer and electronics application. In classical logic, an object takes on a value of either 0 or 1 .In fuzzy logic, a statement can assume any real value between 0 and 1, representing the degree to which an element belong to given set. Fuzzy set is defined as a set whose elements have degree of membership.

- A fuzzy subset F of a set S can be defined as a set of ordered pairs. The first element of the ordered pair is from the set S, and the 2nd element from the ordered pair is from the interval [0, 1].
- The value zero is used to represent non membership; the value one is used to represent complete membership and the value in between are used to represent degrees of membership.

The common method of representing Fuzzy set is

$$A = \{x, \mu_A(x)\}\ x\ \varepsilon \mathbf{X} \quad (1)$$

Where x is an element in **X** and $\mu_A(x)$ is the membership function of set A which defines the membership of fuzzy set A in the universe of discourse, **X**. [23]

A. Fuzzy inference system

Fuzzy inference system is a process of formulating the mapping from a given input to an output using fuzzy logic. The mapping then provides a basis from which decision can be made or pattern discerned. the process of fuzzy inference involves all the process i.e. Membership function, logical operations, fuzzification , defuzzification and if –then rules. Fuzzy inference systems have been applied successfully in fields such as automatic control, data classification, decision analysis, expert system and computer vision.[23]

Basically, fuzzy inference system consists of five functional blocks as shown in Figure III.1

- A **rule base** containing a number of fuzzy if –then rules;
- A **database** which defines the membership functions of fuzzy sets used in the fuzzy rules;
- A **decision making unit** which perform inference operation on the rules.
- A **fuzzificationinterface** which transforms the crisp inputs in to degree of match with liguistic values;

A **defuzzification interface** which transform the fuzzy results on the interface in to a crisp output

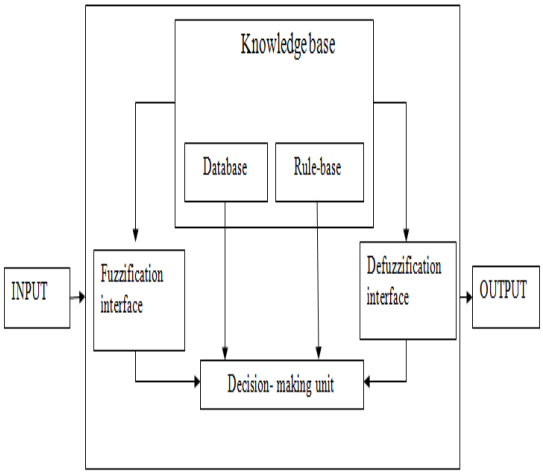

Figure III.1 Fuzzy inference system

Steps performed by Fuzzy inference system are:

1. Compare the input variables with the membership functions on the premise part to obtain the membership values of each linguistic label.
2. Combine the membership values on the premise part to get weight of each rule.
3. Generate the qualified consequent of each rule depending on the firing strength.

Aggregate the qualified consequents to produce a crisp output.

B. Fuzzy membership functions

- **Triangular membership function**

  It is a special case of linear representation. Triangular membership function is represented by a triplet notation x□ □<a,b,c>.triangular membership function is defined as :

$$\mu_A(x) = \begin{cases} 0, \text{for } x < a \\ \frac{x-a}{b-a}, \text{ for } a \le x \le b \\ \frac{c-x}{c-b}, \text{ for } b \le x \le c \\ 0, \text{ for } x > c \end{cases} \quad \text{.....(2)}$$

- **Trapezoidalfunctions**

  It is defined by four parameters, x <a,b,c,d>. A trapezoidalfunction formally described by

$$\mu_A(x) = \begin{cases} 0, \text{ for } x < a \\ \frac{x-a}{b-a}, \text{for } a \le x \le bv \\ 1, \text{ for } b \le x \le c \\ \frac{d-x}{d-c}, \quad \text{forc} \le x \le d \end{cases} \quad \text{.....(3)}$$

- **Normalized Gaussian functions**

  It is another fuzzy membership function that isoften used to represent vague, linguistic terms is the Gaussian which is defined by two parameters
  x<σ,c>, is represented by :

$$\mu_A(x) = e^{-(x-c)^2 / 2\sigma^2} \quad (4)$$

C. Mamdani Fuzzy models

Mamdani's fuzzy inference method is the most commonly seen fuzzy methodolgy.it was among the first control system built using fuzzy set theory. it was proposed in 1975 by Ebrahim Mamdani.mamdani type inference, expects the output membership functions to be fuzzy sets. after the aggregation process, there is a fuzzy set for each output variable that needs defuzzification.it is possible, and in many cases much more efficient

To use a single spike as the output membership functions rather than a distributed fuzzy set .this type of output known as singleton output membership function and it can be thought as a predefuzzified fuzzy set. it enhance the efficiency of the defuzzification process because it greatly simplifies the computation required by the more general Mamdani method, which finds the centroid of a two dimensional function.[23]..it is well suited to human input and it is intutive due to this property it is more advantageous than sugeno method.

D. Sugeno Fuzzy models

it is also known as Takagi Sugeno- Kang, Method of fuzzy inference. introdued in 1985, it is similar to mamdani method to many respects. The first two parts of fuzzy inference process, fuzzyfying the inputs and applying the fuzzy operator, are exactly the same. the main difference between Mamdani and Sugeno is that the Sugeno output membership function are either linear or constant.it is computationaly efficient and it works well with linear technique

A typical rule in a sugeno model has the form
if input1= x and input 2 = y, then output is z= ax+by+c,
"if x is A & y is B then z = f(x,y)"
where A & B are fuzzy sets in the antecedent, while z= f(x,y) is a crisp function in the consequent

- if f(x,y) is a first order polynomial, then the resulting fuzzy inference is called a first order Sugeno fuzzy model.
- if f(x,y) is a constant then it is a zero order Sugeno fuzzy model(special case of Mamdani model) for a zero order Sugeno model, output level z is a constant (a=b=0).

IV. PROPOSED METHOD

In our proposed method we have taken two components of human body .first component is hand and another component is leg.2nd component is subdivided into toe and heel of both left and right feet. We insert a white dot point on component selected parameters at all frames as shown in figure IV.1 below.

Figure IV.1 White dot points on subject selected parameters

Thesewhite dotted frames of each individual inputted in our gait system, which is designed in MATLAB for gait recognition. Two triangles are created between above features. First triangle is drawn between hand and two heels of both feet (right heel and left heel) and 2nd triangle is created between same hand and two toe of both feet (right toe and left toe).we find two intersecting points between these two triangles and angles at these intersecting points lies between 0 to 180 degrees shown in figure IV.2 below:

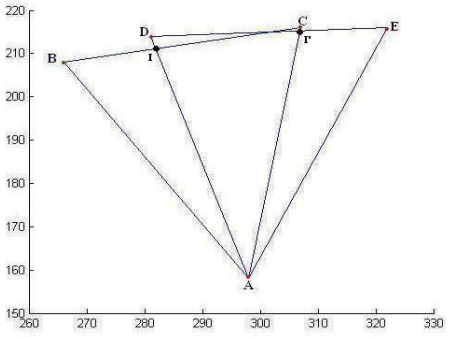

Figure IV.2 I and I' are intersecting points betweenΔ's ABC & ADE.

I ' & I are two intersecting points which have to be computed using parametric line equation and angles at these intersecting points [22].here point A represent Hand and point B,C represents toe of both feet(left and right),point D,C represents heel of both feet(Left and Right) shown in figure IV.2 after that we compute mean values of two angles of an individual subject. After computation of mean values of two angles we take these values as input of our fuzzy inference system .FIS compare these values with the database values and after that FIS produces result according to the fuzzy rule as follows:

- if (Angle 1 is Yes) and (Angle 2 is Yes) Then (match is Excellent) (1)
- if (Angle 1 is No) and (Angle 2 is Yes) Then (match is Average) (1)
- if (Angle 1 is Yes) and (Angle 2 is No) Then (match is Average) (1)
- if (Angle 1 is No) and (Angle 2 is No) Then (match is No match) (1)
- if (Angle 1 is No) and (Angle 2 is No) Then (match is No match) (0)
- if (Angle 1 is Yes) and (Angle 2 is Yes) Then (match is excellent) (0)
- if (Angle 1 is No) and (Angle 2 is Yes) Then (match is Average) (0)
- if (Angle 1 is Yes) and (Angle 2 is No) Then (match is Average) (0)

A. Proposed Algorithm

The Algorithm is designed for gait recognition using mean value of angles and fuzzy logic .fuzzy logic improves our recognition rate and matching accuracy.

1) start
2) input subjects frames
3) Convert frames into grayscale.
4) compute pixel values of desired features i.e.
- *Arm*
- *Right toe and heel*
- *left toe and heel..*

5) construct two triangle between pixel values of these desired features.
6) compute two angles at each intersecting points.
7) find mean value of two angles.
8) input mean values of angles in a fuzzy inference system(FIS).
9) compare FIS(Fuzzy inference system) with the database values.
10) FIS produce results .
11) store result in database.
12) Repeat step 1 to 11 for another subject.
13) End

B. Proposed flow chart

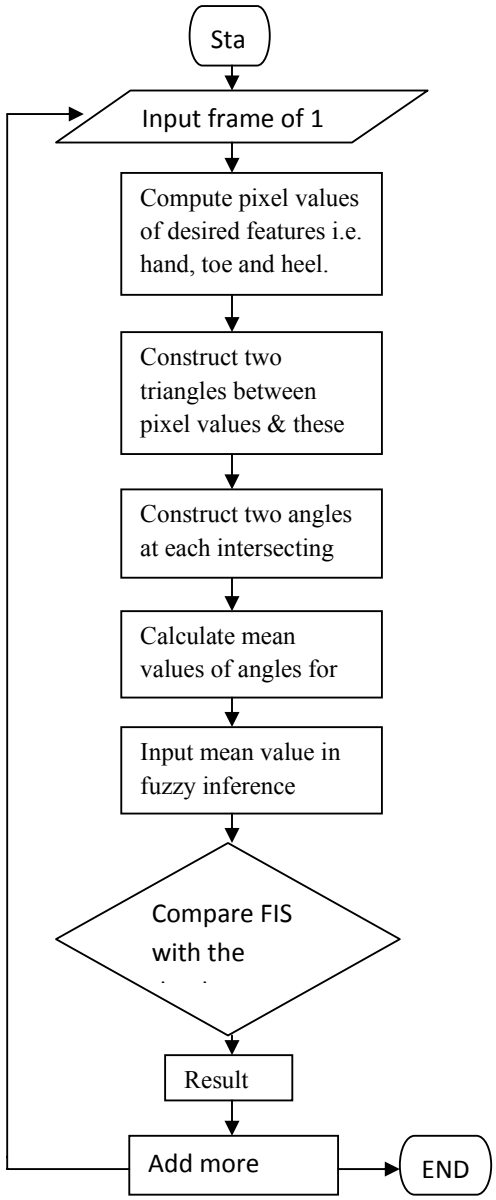

Figure IV.3 Flowchart showing Proposed Gait System

V. EXPERIMENTAL RESULT & ANALYSIS

Our experiments are done on CASIA dataset A[15] for analysis of gait recognition of proposed method. We have taken 17 subjects for gait recognition analysis. We have done gait analysis on gray level images. When we input dotted RGB frames of an individual subjects in our gait system after that these RGB frames are converted in to gray scale for further processing. Only two parameters we have considered out of seven components of human body [7]. Parametric line equation provides better variation in each subject.

Table V.1 shows the results of mean value angles of two angles that we calculated between two triangles intersecting points, created using parametric line equation.

Subjects	Angle 1st mean values	Angle 2nd mean values
A	75.064	86.655
B	78.3647	94.0671
C	77.0836	97.8904
D	80.5067	93.0817
E	82.452	99.2792
F	86.109	103.0987
G	89.2465	101.7519
H	84.6639	103.2414
I	81.4461	97.137
J	82.5426	96.7582
K	72.0027	81.1398
L	87.3647	102.2194
M	84.767	104.8248
N	79.9892	89.244
O	75.4974	86.4331
P	80.7623	92.0858
Q	82.3511	98.7227

Table V.1 Experimental result of first and secondangle mean value of individual subjects

Table V.2 shows that we compare the result with fuzzy logic and without fuzzy logic .the matching accuracy increases with fuzzy logic .

Subjects	Without Fuzzy Logic		With Fuzzy Logic	Values
	Angle 1st mean values	Angle 2nd mean values		
	75.064	86.655		80.043
A	78.3647	94.067	Good	86.537
B	77.0836	97.890	Excellent	83.278
C	80.5067	93.081	Good	84.269
D	82.452	99.279	Good	81.431
E	86.109	103.09	Good	86.536
F	89.2465	101.75	Excellent	79.440
G	84.6639	103.24	Good	77.241
H	81.4461	97.13	Good	86.537
I	82.5426	96.75	Excellent	86.758
J	72.0027	81.13	Excellent	76.139
K	87.3647	102.21	Good	83.657
L	84.767	104.82	Good	82.824
M	79.9892	89.24	Good	75.104
N	75.4974	86.433	Average	80.433
O	80.7623	92.085	Good	77.751
P	82.3511	98.722	Good	81.402
Q			Good	

Table V.2 Experimental result of first and second angle mean value of individual subjects using Fuzzy inference system

Result shown in table V.2 depicts that the mean values of two angles take as an input of fuzzy inference system then fuzzy inference system and it compare with the database .the above results shows

that " matching accuracy lies between 75 to 86 percent ".

Comparison with other Algorithm

Algorithm	CCR
Static body Parameters (Georgia Tech)	73%(18)
Motion based Eigen space analysis(UMD)	75%(44)
Method based on Positioning body joints	78%(118)
Method based on dynamic body Parameters	78%(17)
Proposed method based on dynamic body parameters with fuzzy inference system	75% to 86%(17)

Table V.3 Experimental results compared with other Algorithm

From Table V.3 it can be seen that higher recognition rate has been obtained according to gait recognition method based on the proposed Algorithm.

CONCLUSIONS AND FUTURE SCOPE

In this paper, we have shown a new approach to enhance gait recognition rate with fuzzy logic. It is clear from our experiments that the assumptions made on dynamic features of human body (i.e. hand and feet) increase gait recognition and the average classification. We have used fuzzy logic on mean values of two angles. Due to this, matching accuracy is increases and it lies between 75 to 86 percent. We have done our experiment on CASIA dataset A of 17 subjects. Our result analysis on this dataset gives better recognition rate. our experiment result shows that the concept of fuzzy logic with mean values of both angles gives better gait recognition.

The present study was occurred on the side view of subject gait .similar study can be conducted on different view angle of subject gait. Our study was confined to a sample of 17 subjects of CASIA dataset. Similar work can be conducted on more sample database of different organization for result analysis.

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MATHEMATICAL MODEL OF INFORMATION AND A NEW APPROACH OF CODING IN IT

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Abstract:- In this paper we are discussed about logical sentence coding for distinct messages by binary alphabets {0, 1}.The information model contains alphabets, words, sentences and messages are available in the practical purpose. The information and its relation discussed for clarification.

Keywards :- Logical Information ,Partial Sum.

I. INTRODUCTION

In our discussion of the paper is that alphabet is the binary alphabet {0,1}. A code is also collection of logical sentence that are used to be represent distinct messages .A sentence in a code is also called a *code-sentence*. Suppose a logical sentence is transmitted from its source of information to its destination. In case of transmission, *inferences* such as noises might cause some of the 1's in the code-sentence to be received as 0's and some of the 0's to be received as 1's.There fore received sentence might no longer supposed as the transmitted one and that one is our aim to recover that transmitted sentence if at every case of possible.

Generally, in telephone wires strung between poles ,later the were cables on poles and in trenches .Next come microwave between relay towers on hill tops follow the were less communication system. Subsequently joined by microwave beam to and from satellites and fix points high wave equator. Now more and more long lines are *fiber-optic* cables. The microwave towers are spaced at 26 mile intervals in long chains that join cities. They are followed the *logical communication system* (LCS).

II. LOGICAL INFORMATION CODING

In modern communication system ,data items are constantly being transmitted from point to point .The basic unit of information called a message, is a finite sequence of character that we want to transmit is now represented as a sequence of m-elements from A .Choose our alphabet set A={0,1}.Let A^m denote the binary sequence of length n. Let $\hat{+}$ be a binary operation on A such that for x and y in A. Then $x \hat{+} y$ is called *partial sum* of sequence length n means carry part is neglected during addition and one if both are different. For example

X=10101 and y=10011 then $x \hat{+} y$ is 00110

To show that (A^m ,$\hat{+}$) is a group by using the properties.

Let x be a sentence in A. We define the weight of x denoted by ω(x) to be the number of 1's in x. The weight of 00110 is two. We define the weight of x and y denoted by ω(x,y) to be the weight of $x \hat{+} y$ is ω(x,y) . Note that the *partial sum* of two words is exactly carry part is neglected during sum and one if both are different . We establish a theorem as follows.

THEOREM:-2.1.

Let x,y and z be elements of A^m . Then

(a) $\omega(x,y) = \omega(y,x)$.
(b) $\omega(x,y) \geq 0$.
(c) $\omega(x,y) = 0$ if and only if x=y.
(d) $\omega(x,y) \leq \omega(x,z) \hat{+} \omega(z,y)$.

PROOF:- The first three properties are simple to prove are not needed.

(d). For x,y in A^m , $|x \hat{+} y| \leq |x| \hat{+} |y|$

If $x \in A^m$, then $x \hat{+} x = \bar{o}$, the identity element in A^m .

Then $\omega(x,y) = |x \hat{+} y| = |x \hat{+} \bar{o} \hat{+} y|$
$= |x \hat{+} z \hat{+} z \hat{+} y|$
$\leq |x \hat{+} z| \hat{+} |z \hat{+} y|$
$= \omega(x,z) \hat{+} \omega(z,y)$.

Thus this establishes the theorem.

The transmission of information is to reduce the likelihood of receiving a sentence that differs from the sentence that was sent, the code sentence by means of a transmission channel. Then each code sentence x=e(a) is received as the sentence in A^m . This is received from each $a \in A^m$. e is a function and a may be identified. The noiseless or noiseful arises during transmission.

III. MATHEMATICAL MODEL OF INFORMATION

As we observed that the information can be represented in either symbols , wards ,sentences and message form .The common syntax of representing any information is a mathematical expression .The different models are available in t-he practical purpose .We suggest a triplet (Σ,δ,0) for this purpose.

The symbols Σ, δ and 0 are used for the representation of a set of characters, transactions or relationship from any subset of Σ^* to Σ^* (set of all regular expressions defined on Σ) and the set of operations (logical, arithmetical etc) the following proposition assures the encoding of information with this formulation .

PROPOSITION:-3.1

The set of all alphabets ,words ,sentences and messages are contained in the system (Σ,δ,0).

PROOF:-

Let the system (Σ , δ ,0) be denoted as S .where Σ is the set of alphabets, δ the transactions and 0 is a specific operations on the set of alphabets ,Suppose 0 is the concatenation operation, δ is the identity transformation ,then

$a\ 0\ \lambda = \lambda\ 0\ a = a$ for $a \in \Sigma$

To verify the set of words belongs to S ,the transaction functions are to be considered from any subset of Σ^* to Σ^* and the operation 0 is the concatenation operation.

To show the set of sentences and messages belongs to the system (Σ , δ,0),the choices of δ and 0 should be specific. In this case the operation 0 can be any logical operations such as NOT,AND,NAND,NOR and EOR ,Implication etc.[]

EXAMPLE:-3.2

The sentence "This white car is mine" belongs to the information system (Σ , δ,0). In this case Σ is the set of all English characters including the blank character 'b' and the null characters " lambda" the transaction function δ is a mapping from subset of Σ^* to Σ^* such that δ(this white car is mine)= thiswhitecarismine. This string is a word in Σ^*.

If T ={b,a,c,e,h,I,m,n,r,s,t,w}, $\delta: T \rightarrow \Sigma^*$ then for $u \in \Sigma^*$ such that
u={t,th,thi,this,thisb,thisbw,thisbwh,thisbwhi,thisbwhit,thisbwhite,thisbwhiteb,
thisbwhitebc,thisbwhitebca,thisbwhitebcar …… }

So 0 is the recursively concatenation operation.

IV. MESSAGE REPRESENTATION

Usually message are represented either in the sequential coding or in the alpha numeric forms. The communication protocols use different types of coding as per the data transmission equipments infrastructures and the security to the data contents. Most of the communication systems use sequential coding. One of the data transmission permission is obtained from the receiver 's end within the STX(start of text)and ETX(end of text) commands most of the massages are transmitted through the proper code. In fact, the codes are binary characters. *Telephone network,Cable television network and Computer network etc*, use binary codes for the data transmission, Surface mail (i.e., News paper etc.) or postal messages are encoding in any other type of characters, not necessarily binary codes.

V. INFORMATION AND ITS RELATIONSHIP WITH MESSAGE

Message carry information. All information derived from any message are either correct or wrong. The information can be interpreted as the proposition or predicates. The sentence connectors and parsers can degenerate information from the basic literal associated with the message.

VI. CONCLUSION

This paper gives the details clarification of different messages during transmission. The transmission of information from point to point and its basic unit called message. The *Telephone network, Cable television network and Computer networks etc*. use binary codes during data transmission. The binary coding is used in this paper is easily implemented in the personal computer system. The messages are either correct or wrong is identified by the system.

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DESIGN AND SIMULATION OF A NEW 2-DIMENSIONAL TRANSFORM TECHNIQUE FOR SINUS ARRHYTHMIA PATIENT'S ELECTROCARDIOGRAM SIGNAL COMPRESSION

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Abstract— Electrocardiogram signal compression algorithm is needed to reduce the amount of data to be transmitted, stored and analyzed, without losing the clinical information content. In this work takes the real time data of the Sinus Arrhythmia patient and investigates a set of ECG signal compression schemes to compare their performances in compressing Sinus Arrhythmia patient's ECG signals. These schemes are based on transform methods such as discrete cosine transform (DCT), fast Fourier transform (FFT), discrete sine transform (DST), and their improvements. An improvement of a discrete cosine transform (DCT)-based method for electrocardiogram (ECG) compression is also presented as DCT-II. A comparative study of performance of different transforms is made in terms of Compression Ratio (CR) and Percent root mean square difference (PRD).The appropriate use of a block based DCT associated to a uniform scalar dead zone quantiser and arithmetic coding show very good results, confirming that the proposed strategy exhibits competitive performances compared with the most popular compressors used for ECG compression. Each specific transform is applied to a pre-selected data segment from the CSE database, and then compression is performed.

Keywords— *Compression Ratio, Compression factor, Compression time, ECG, PRD.*

I. INTRODUCTION

An ECG signal is a graphical representation produced by an electrocardiograph, which records the electrical activity of the heart over time. The ambulatory monitoring system usually requires continuous 12 or 24-hours ambulatory recording for good diagnostic quality. For example, with the sampling rate of 360 Hz, 11 bit/sample data resolution,
a 24-h record requires about 43 MByte per channel. So, 12-channel system requires nearly 513.216 M-Byte of storage disks daily.

Because of the tremendous amount of ECG data generated each year, an effective data compression schemes for ECG signals are required in many practical applications including ECG data storage or transmission over telephone line or digital telecommunication network. ECG data compression techniques are typically classified into three major categories; namely direct data compression [3]-[4], transform coding [5]-[8], and parameter extraction methods [9]-[11]. The direct data compression methods attempt to reduce redundancy in the data sequence by examining a successive number of neighboring samples. These techniques generally eliminate samples that can be implied by examining preceding and succeeding samples. Even though many compression algorithms have been reported so far in the literature, not so many are currently used in monitoring systems and telemedicine.

In this paper a new compression technique asked on transform coding-II and QRS complex estimation is proposed. There are two motivations in this work. The first motivation is the QRS complex estimation using the extraction of significant features of ECG waveform. The second motivation is the selection of the threshold levels in each sub band such that high CR and low PRD are obtained. The significant features of ECG waveform are extracted to estimate the QRS complex. Then, the estimated QRS-complex is subtracted from the original ECG signal. After that, the resulting error signal is discrete cosine transformed and the coefficients are threshold based on the energy packing efficiency. Finally the significant coefficients are coded and stored or transmitted.

II. FEATURE EXTRACTION OF ECG SIGNAL

It has now gone beyond the capacity of the expert cardiologist to take care of large numbers of cardiac patients efficiently & effectively. Therefore, computer- aided feature extraction and analysis of ECG signal for disease diagnosis has become the necessity. The first step in computer aided diagnosis is the identification & extraction of the features of the ECG signal. The QRS complex is the most prominent feature and its accurate detection forms the basis of extraction of other features and parameters from the ECG signal. There are a number of methods, some of which deal with detection of ECG wave segments, namely P, QRS and T, while others deals with

detection of QRS complexes. A good amount of research work has been carried out during the last five decades for the accurate and reliable detection of QRS segment in the ECG signal. The QRS detection algorithms developed so far can be broadly placed into four categories: (i) Syntactic approach (ii) Non-Syntactic approach (iii) Hybrid approach and (iv) Transformative approach.

[A] Syntactic Approach:
The syntactic approach is basically pattern recognition based QRS detection techniques. The ECG signal is first reduced into a set of elementary patterns like peaks, durations, slopes, interwave segments and thereafter use rule based grammar. The signal is represented as a composite entity of peaks, duration, slopes and interwave segments. These patterns are then used to detect the QRS complexes in the ECG signal. These methods are time consuming and require inference grammar in each step of execution for QRS detection.

[B] Non-syntactic Approach:
Non-syntactic type is the most widely used class of ECG feature extraction techniques. In this class, we find the use of amplitude, slope and threshold limit as well as the use of different filters, mathematical functions and models. Okada reported a five step digital filter, which removes components other than those of QRS complex from the recorded ECG [24]. The final step of the filter produces a square wave and its on-intervals correspond to the segments with QRS complexes in the original signal.

[C] Hybrid Approach:
In hybrid approach, the syntactic and non-syntactic approaches are combined to detect the QRS complex. These are not in common use, as in syntactic approach, the trace is being made on actual morphology of the ECG signal and in non-syntactic approach; there is no consideration to maintain the morphology of the ECG signal.

[D] Transformative Approach:
Transformative Techniques, namely Fourier Transform, Cosine Transform, Pole –zero Transform, Differentiator Transform, Hilbert Transform and Wavelet Transform are being used for the QRS detection. The use of these transforms on ECG signal helps to characterize the signal into energy, slope, or spike spectra, and thereafter, the temporal locations are detected with the help of decision rules like thresholds of amplitude, slope or duration. Murthy and Prasad proposed a solution to the fundamental problem of ECG analysis, viz., delineation of the signal into its component waves [25].

III. COMPRESSION TECHNIQUES

Lossless compression algorithms: the Run Length Encoding Algorithm, Huffman Encoding Algorithm, Shannon Fano Algorithm, Lempel Zev Welch Algorithm, Discrete Cosine Transform, Fast Fourier Transform, Discrete Sine Transform and Discrete Cosine Transform-II are implemented and tested with a set of ECG signal. Performances of the compression methods are also evaluated at the end of the paper.

[A] Run Length Encoding
Run Length Encoding or simply RLE is the simplest of the data compression algorithms. The consecutive sequences of symbols are identified as runs and the others are identified as non runs in this algorithm. This Algorithm deals with some sort of redundancy [4]. It checks whether there are any repeating symbols or not, and is based on those redundancies and their lengths.

[B] Huffman fano Approach:
Huffman fano Algorithms calculate the frequencies first and then generate a common tree for both the compression and decompression processes [5]. Huffman Encoding and Shannon Fano approaches are implemented and executed independently.

[C] Discrete Cosine Transform (DCT):
A discrete cosine transform (DCT) [19] expresses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies [9]. Discrete Cosine Transform is a basis for many signal and image compression algorithms due to its high de-correlation and energy compaction property [10].

[D]Fast Fourier Transform (FFT):
A fast Fourier transform (FFT) [11] is an efficient algorithm to compute the discrete Fourier transforms (DFT) and it's inverse [12]. An FFT is a way to compute the same result more quickly. Computing a DFT of N points in the naive way, using the definition, takes $O(N^2)$ arithmetical operations [13], while an FFT can compute the same result in only O(N log N) operations. Fast Fourier Transform is a fundamental transform in digital signal processing with applications in frequency analysis, signal processing etc [10]. The periodicity and symmetry properties of DFT are useful for compression.

[E] Discrete Sine Transform (DST):
Discrete sine transform (DST) [14] is a Fourier-related transform similar to the discrete Fourier transform (DFT), but using a purely real matrix. DST implies different boundary conditions than the DFT or other related transforms [15].

[F]Proposed Method (DCT-II):
The most common variant of discrete cosine transform is the type-II DCT [16]. The DCT-II is typically defined as a real, orthogonal (unitary), linear transformation. DCT-II can be viewed as special case of the discrete Fourier transform (DFT) with real inputs of certain symmetry [17]. This viewpoint is fruitful because it means that any FFT algorithm for the DFT leads immediately to a corresponding fast algorithm for the DCT-II simply by discarding the redundant operations.

IV. PERFORMANCE EVALUATION

Depending on the nature of the application there are various criteria to measure the performance of a compression algorithm [18]. Following are some measurements used to evaluate the performances of lossless algorithms.

5.1 Compression Ratio (CR):
Compression ratio is the ratio between the size of the compressed file and the size of the source file [23].

$$\text{Compression Ratio} = \frac{\text{size after compression}}{\text{size before compression}} \quad (1)$$

5.2 Compression factor (CF):
It is the inverse of the compression ratio. That is the ratio between the size of the source file and the size of the compressed file.

$$\text{Compression Factor} = \frac{\text{size before compression}}{\text{size after compression}} \quad (2)$$

5.3 Percent root mean square difference (PRD):
PRD is the most prominently used distortion measure is the Percent Root mean square Difference (PRD) [18] that is given by

$$PRD = \left[\frac{\sum_{n=1}^{Lb}[x(n)-x'(n)]^2}{\sum_{n=1}^{Lb}[x(n)]^2}\right]^{(1/2)} \quad (3)$$

where x(n) is the original signal, x'(n) is the reconstructed signal and Lb is the length of the block or sequence over which PRD is calculated. PRD provides a numerical measure of the residual root mean square (rms) error.

5.4 Compression Time (CT):
It is defined as the total time elapsed during the compression of original ECG signal. If the compression and decompression times of an algorithm are less or in an acceptable level it implies that the algorithm is acceptable with respective to the time factor. With the development of high speed computer accessories this factor may give very small values and those may depend on the performance of computers.

V. RESULTS AND DISCUSSION

Physiobank ATM database has been used to test the performance of the compression techniques. The ECG data is sampled at 250 Hz. The amount of compression is measured by CR and the distortion between the original and reconstructed signal is measured by PRD. The comparison table shown in Table 1, details the resultant compression techniques. This gives the choice to select the best suitable compression method. A data compression algorithm must represent the data with acceptable fidelity while achieving high CR. As the PRD indicates reconstruction fidelity; the increase in its value is actually undesirable. Although proposed method provides maximum CR, but distortion is more. So a compromise is made between CR and PRD.

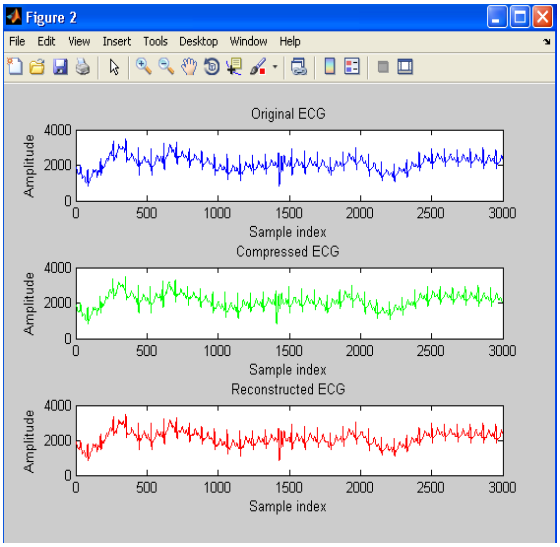
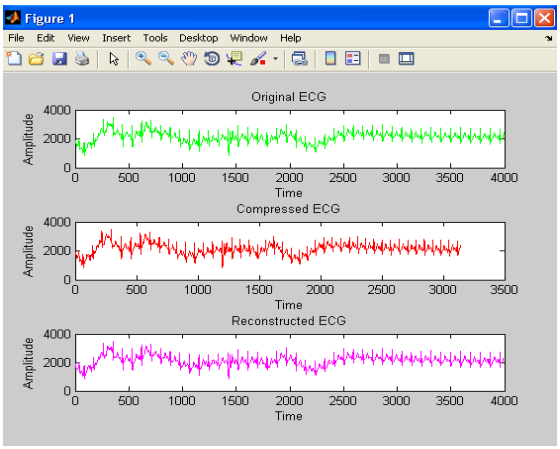


Figure 1. Result of the Sinus Arrhythmia patient's ECG signal compressed by



RLE Algorithm

Figure 2. Result of the Sinus Arrhythmia patient's ECG signal compressed by FAN Algorithm

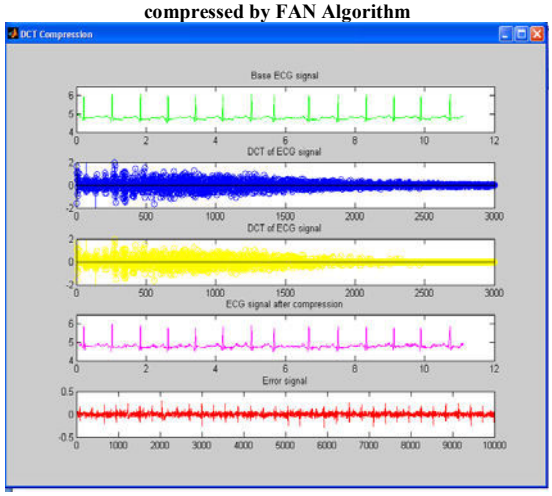


Figure 3. Result of the Sinus Arrhythmia patient's ECG signal compressed by DCT Algorithm

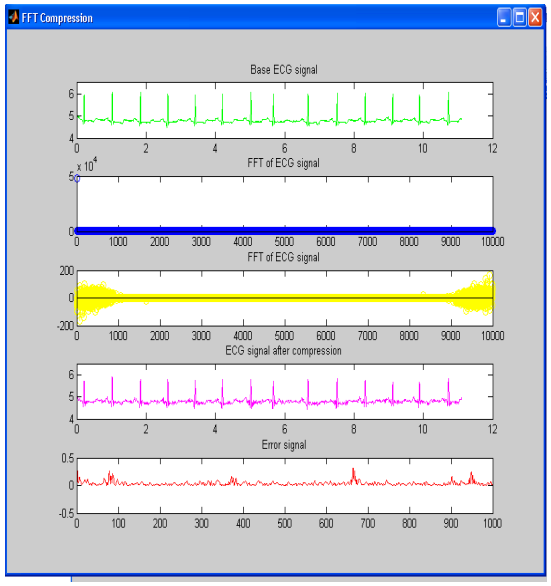


Figure 4. Result of the Sinus Arrhythmia patient's ECG signal compressed by FFT Algorithm

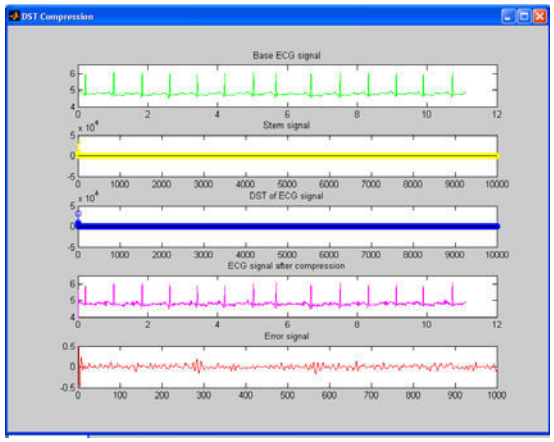


Figure 5. Result of the Sinus Arrhythmia patient's ECG signal compressed by DST Algorithm

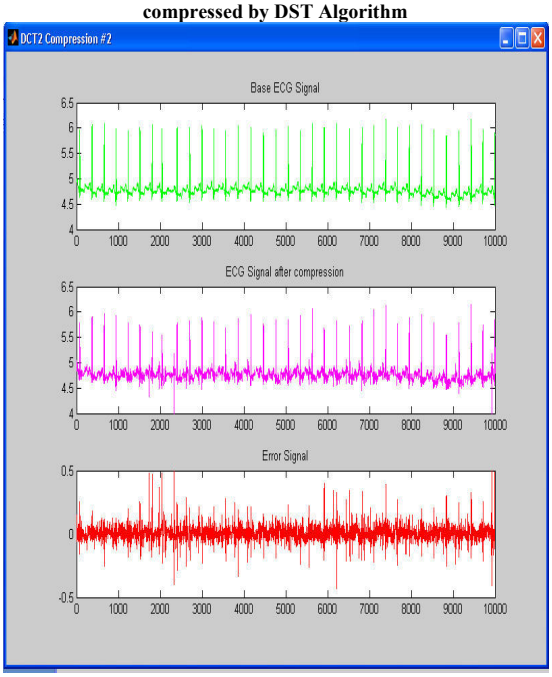


Figure 6. Result of the Sinus Arrhythmia patient's ECG signal compressed by proposed DCT-II method.

Method	CR	CF	PRD	CT
RLE	98.67	0.01013	2.4216	0.582020
FANO	78.58	0.01272	0.5044	0.163039
DCT	90.43	0.01105	0.9382	5.430610
FFT	89.57	0.01116	1.1661	5.451094
DST	85.18	0.01173	1.2589	5.461161
Proposed	**95.77**	**0.01044**	**1.3319**	**0.512942**

Table. Comparison table for the Performance of Compression Techniques

VI. CONCLUSION

Among the six techniques presented, Fano provides lowest CR but distortion is low. Next is DST which gives higher CR 85.18 with PRD as 1.2589. FFT gives higher CR as 89.57 but PRD is high as 1.1661 But DCT-II provides an improvement in terms of CR of 95.77 and PRD is also low as 1.3319. Thus an improvement of a discrete cosine transform (DCT)-based method for electrocardiogram (ECG) compression is presented as DCT-II in terms of amount of compression. The appropriate use of a block based DCT-II associated to a uniform scalar dead zone quantiser and arithmetic coding show very good results, confirming that the proposed strategy exhibits competitive performances compared with the

most popular compressors used for ECG compression.

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DEVELOPMENT OF ECG SIGNAL COMPRESSION ALGORITHM USING DISCRETE-COSINE-TRANSFORMATION

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Abstract— In this work, an algorithm has been developed to compress electrocardiograms (ECG) acquired from normal individuals using POLYPARA Laptop. The developed algorithm comprises discrete-cosine-transform (DCT) technique followed by Huffman encoding and decoding. The DCT coefficients are thresholded. Then inverse DCT is performed. The percentage root mean square difference (PRD) is calculated from the reconstructed signal. The binary look up table is created by the thresholded DCT coefficients which is then encoded and decoded by the Huffman coding. Finally, the compression ratio (CR) is calculated. The algorithm has been developed on MATLAB platform.

Keywords- Compression Ratio (CR); Discrete-Cosine-Transform (DCT); Electrocardiograms (ECG); Huffman encoding and decoding; Percentage Root Mean Square Difference (PRD)

I. INTRODUCTION

Biological signal, especially ECG has an important role in diagnosis of heart diseases. Therefore, ECG processing has been a topic of great interest and is most commonly used in application such as monitoring heart's condition. Long term records are needed to extract or detect important information from the heart signal. Hence, ECG data compression has utmost importance to reduce storage requirements and/or the transmission rate for remote monitoring and diagnosis and archiving. A number of lossy ECG compression techniques have been proposed in the literature. These mainly fall into two categories: (i) Direct compression [1] such as Amplitude-Zone-Time Epoch Coding (AZTEC) method, the Coordinate Reduction Time Coding System (CORTES), Turning Point (TP) technique, Scan-Along Polygonal Approximation (SAPA), peak-picking, cycle-to-cycle, Differential Pulse Code Modulation (DPCM) and the Long-Term-Prediction (LTP) and (ii) Transformational methods [2] such as Fourier transform, Walsh transform, Karhunen-Loeve Transform (KLT), discrete cosine transform (DCT) [3-4] and Wavelet transform (WT). In most cases, it is found that the direct methods are superior than the transform based methods with respect to system simplicity and error. On the contrary, the transform methods achieve higher compression ratio.

This paper introduces one of the transformational methods of lossy compression that is the idea of discrete cosine transform (DCT) on ECG signal compression. The ECG signal is acquired through the POLYPARA laptop from normal subjects. Performance evaluation parameters are explained in section II. The transformational method is discussed in section III. The signal is then compressed which is discussed under section IV. Finally, results and concluding remarks are discussed under section V and VI respectively.

II. PERFORMANCE EVALUATION PARAMETERS

A. Compression Ratio (CR)

One of the important compression measuring parameter is the compression ratio. It is given by the ratio of the length of the original data to the length of the compressed data. It is given by, CR=K/P where 'K' is the length of the original data and 'P' is the length of the compressed data [1-3].

B. Percentage-of-root-mean-square-difference (PRD)

PRD is also another performance evaluation parameter to detect the compression of the ECG signal [5]. It is the rate of difference between the original and the reconstruction. It is used to determine the efficiency of a compression algorithm. The PRD is calculated as:

$$PRD=\sqrt{\frac{\sum(x_i-y_i^2)}{\sum x_i^2}}\times 100 \quad (1)$$

where 'x_i' is the original signal and 'y_i' is its reconstructed version.

III. DISCRETE COSINE TRANSFORM (DCT)

The one dimensional DCT of a sequence x(n) [6-8] is given by,

$$C(k)= \alpha(k)\sum_{n=0}^{N-1} x(n)\cos\left(\frac{\pi(2n+1)k}{2N}\right), 0 \le n \le N-1, \quad 0 \le k \le N-1 \quad \text{.....(2)}$$

where $\alpha(0) = \sqrt{\frac{1}{N}}$ for k=0 and $\alpha(k) = \sqrt{\frac{2}{N}}$ for $1 \le k \le N-1$.
The inverse DCT is defined by,

$$x(n) = \sum_{k=0}^{N-1} \alpha(k) C(k) \cos\left(\frac{\pi(2n+1)k}{2N}\right), 0 \le n \le N-1 \quad \text{.....(3)}$$

IV. METHOD

The developed algorithm comprises of the following steps.
Step1: At first, the ECG signal (after removing its mean value) is transformed by means of the DCT transform.
Step 2: A copy of transformed coefficients (TC) is taken and it is thresholded by, TH= (THmin + THmax)/2
Step 3: Inverse DCT (IDCT) is applied on the DCT coefficients.
Step 4: PRD is then computed.
Step 5: Binary look-up table is then constructed to represent the zero and non-zero coefficients obtained after thresholding in step 2. Here, the non-zero DCT coefficients are located sequentially by 1's. This binary table is encoded and decoded using the Huffman coding.
Step 6: The length of the compressed and decompressed data are checked and the compression ratio is calculated.

Before computing the PRD, it is to be noted that the mean value already subtracted is added to both the zero-mean original and the reconstructed signal obtained after performing the IDCT.

V. RESULTS AND DISCUSSIONS

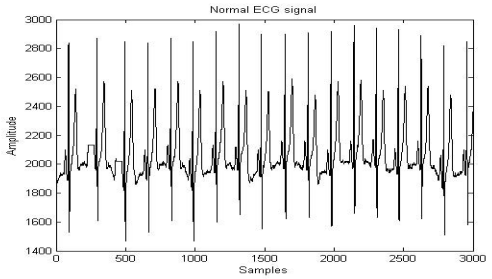

Figure 1: Normal ECG signal

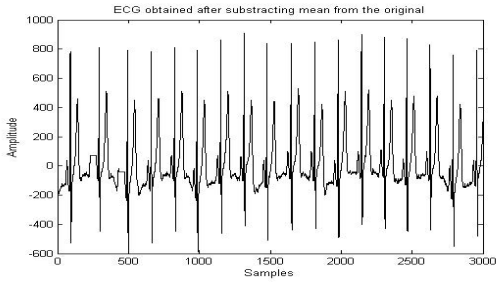

Figure 2: Zero-mean version of original ECG signal

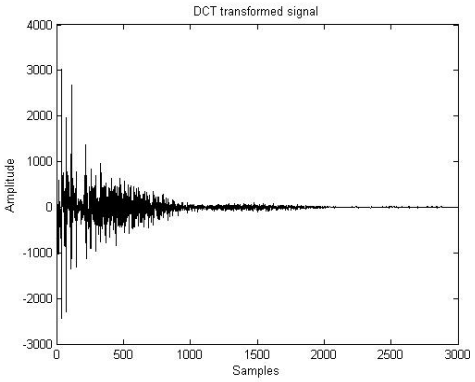

Figure 3: DCT of Zero-Mean ECG signal

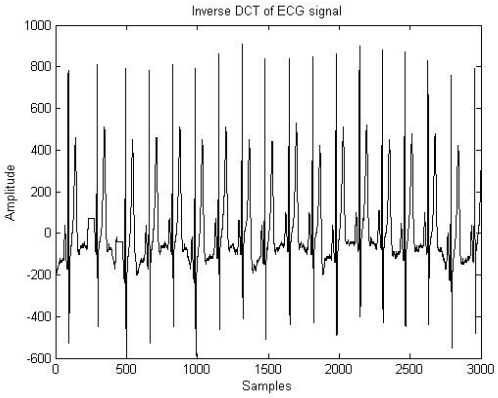

Figure 4: Inverse DCT performed on the DCT transformed signal

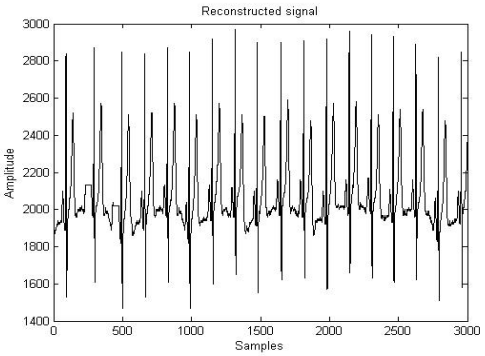

Figure 5: Reconstructed signal after adding mean

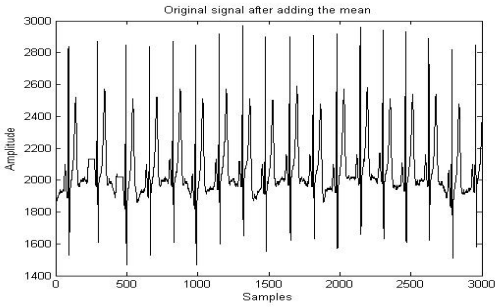

Figure 6: Original signal after adding mean

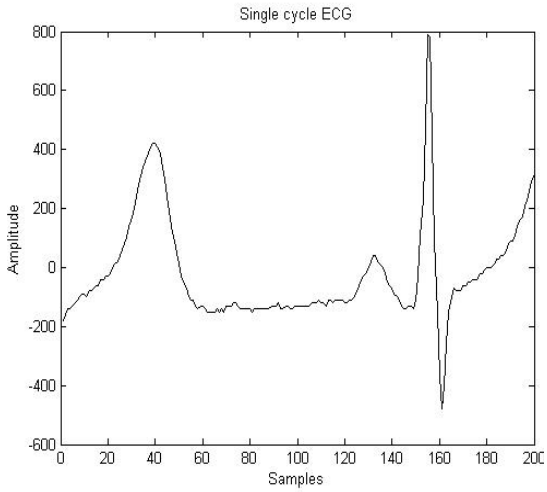

Figure 7: Single cycle zero-mean ECG signal

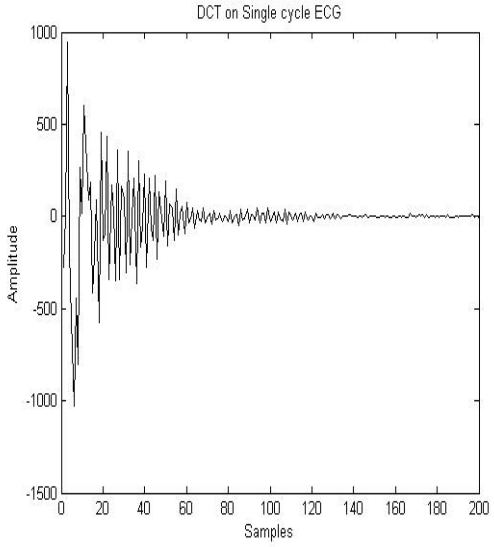

Figure 8: DCT of a zero-mean single cycle ECG signal

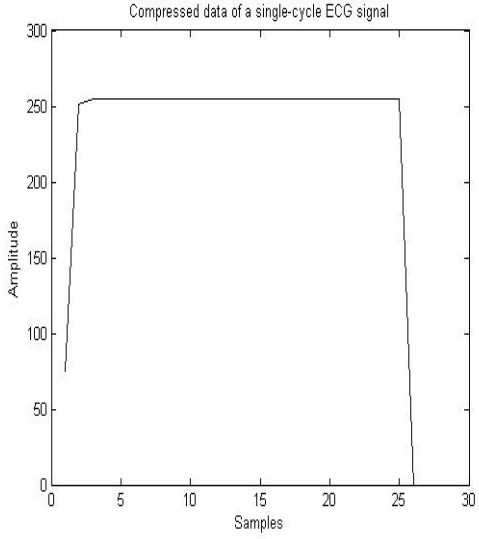

Figure 9: Compressed data of single-cycle ECG signal

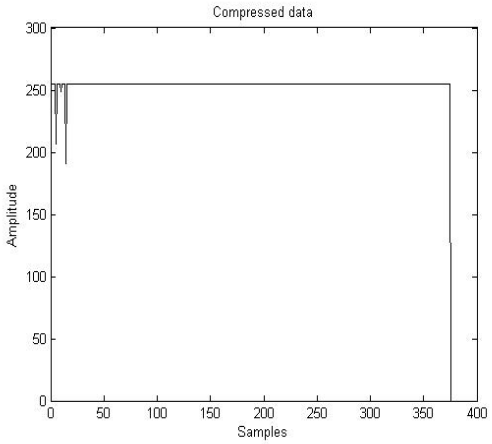

Figure 10: Compressed data of the normal ECG signal

TABLE 1: Performance of DCT

ECG records	CR	PRD(%)
Subject 1	7.9787	57.8497
Subject 2	7.9787	57.8497
Subject 3	7.9787	35.6859
Subject 4	7.9787	105.9719
Subject 5	7.9787	35.3391

The electrocardiograms (ECG) are acquired from five normal subjects using POLYPARA Laptop. 'Fig 1' shows the normal ECG signal of subject 2 shown as a sample case. 'Fig 2' shows the zero-mean version of the original ECG signal. 'Fig 3' shows the DCT of the zero-mean version of the original ECG signal. 'Fig 4' shows the inverse DCT of the signal as per the developed algorithm. 'Fig 5' shows the reconstructed signal after adding the mean. 'Fig 6' shows the original signal obtained after adding the mean. 'Fig 7' shows the single cycle zero-mean ECG signal. It contains 200 samples in one cycle. 'Fig 8' shows the DCT of a single cycle zero-mean ECG signal. 'Fig 9' plots the compressed data of a single-cycle ECG signal, which is done here through the Huffman coding. 'Fig 10' plots the compressed data of the multi-cycle ECG signal, which is done here through the Huffman coding. 'TABLE 1' shows the performance evaluated on the basis of PRD and CR. The reconstructed signal (shown in 'Fig 5') obtained after doing IDCT resembles the original signal (shown in 'Fig 6'). The values of PRD are different for different ECG signals taken in this work.

VI. CONCLUSION

The algorithm developed in this work has given consistent results and it has compressed ECG signals appreciably.

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CONCEPT OF GUARDIAN BEES TO IMPROVING EFFICIENCY OF ARTIFICIAL BEE COLONY ALGORITHM BASED ON THE SHARING FUNCTION IN DYNAMIC ENVIRONMENT

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Abstract—Artificialbee colony optimization algorithm is based on swarm intelligence which has been inspired from bee foraging behavior in nature. The efficiency and the effect of this algorithm have been proved on some static subjects but most of the real world problems are dynamic means that the status and optimized level changes during the time. Shayganpour presented a model of artificial bee colony algorithm in dynamic environment which by assessing this algorithm and due to dynamic environment properties, we improve the efficiency of the algorithm through adding some components. In the current study, we introduce guardian bees and survey their performance and effect on the algorithm efficiency.

Keywords: Dynamic Optimization, Swarm intelligence, Artificial Bee Colony Algorithm, Sharing Function, Guardian bees

I. INTRODUCTION

Nowadays the use of natural concepts to solve complicated optimization problems is common. The reason of such a use is the shortage of classic algorithms for solving large scale and non-linear problems. Swarm intelligence is the collective behavior of decentralized, self-organized systems, natural or artificial. The concept is employed in work on artificial intelligence. Examples of systems that work based upon the Swarm intelligence include ant colonies, bird flocking, animal herding, bacterial growth, and fish schooling.

Most of the issues in which we look for the whole optimization and called finding-optimization issues, are presented statically, while in real world issues have dynamic nature, i.e. with going by the time in direction of finding-optimization, some changes occur in the finding-optimization's issue or limitation of which. If this change occurs, comparing the solution with the former solution is necessary.Therefore, it is better to have a findingoptimization algorithm in order to can deal with the changing environment continuously and use previously results again. The main problem with algorithms in a dynamic environment is that they finally lead to a convergent optimum.

Among Swarm algorithms, the algorithms inspired from bee show acceptable fitness due to the features such as division of labor and different interactions especially in the static environments. Shayganpur [9] presented a model in which she has dealt with the artificial bee colony algorithm by means of sharing process, preventing of algorithms convergence and maintaining variety during the performance, acceptable efficiency and excitability in dynamic environments. In this essay by adding some elements to the name of guardian bees, we try to improve the efficiency of these algorithms. Adding guardian bees to the algorithm prevent reinvestigating areas where they have been tried before and also the areas with high possibility of possessing the peak has been spotted. Accordingly, efficiency of algorithms will improve.

The rest of this essay is organized as: section 2 deals with the describing bees' behavior in nature and identifying the suggested algorithms. Section 3 contains carried out experiments and their results and the final section is conclusion.

II. BEES' COLONY IN NATURE

Bees' colony in nature [5] includes two components: food sources and Forager bees. Forager bees (population) are of two kinds: unemployed and worker bees. Unemployed bees have two categories: scouts and onlookers. Scouts begin the search without prior knowledge and accidentally and onlookers go to the dance floor and begin their search by waggle dance of bees in the dance floor.

The second group includes worker bees. Once anonlookers finds a food source, promotes and turns into a worker bee and remembers the place of food source and flies to it, picks some of the nectar and returns to the hive. Now:

- If the amount of nectar decreases to a low level, bee will leave the food source and turn into an unemployed bee.
- If there is enough nectar in the food source, worker bee can keep on its Foraging without exchanging information and come back to the source.
- If there is enough nectar in the food source, worker bee can exchange information in the dance floor.

The most important part of a hive is the place of exchanging information which is called dance floor. Communication between bees about the quality of food sources is done via waggle dance. Scouts also share their information commensurate with the

quality of food sources. In fact, sharing such information during waggle dance takes more time, so the number of allocated bees to each source is commensurate with the quality of the sources.

III. ARTIFICIAL BEE COLONY ALGORITHM BASED ON SHARNG FUNCTION

In this algorithm the colony contains 3 groups of bees including workers, onlookers, and scouts. The first half of the hive contains artificial worker bees and the second half contains onlooker ones and there is only one worker for each source. In other words, the number of workers is equivalent to the number of sources. When workers faced with an abandoned source, turn into a scout one. Searching in the algorithm of artificial bees' colony is done as the following [7, 6]:

• Worker bees search a food resource next to food resource on their memory (previous solution), in other words, searching for better solution, they correct themselves according to the formula (1):

$$v_{ij} = x_{ij} + \varphi_{ij}\left(x_{ij} - x_{kj}\right) \text{.....(1)}$$

where k Є {1,2,3,…,SN} and i ≠K and φ is a random number within the range of [-1,1], and j Є {1,2,3,…,D}. SN is the number of bees. K is produced randomly and should be different with i; the less the difference between x_{ij} and x_{kj}, the less deviation from x_{kj} situation. In this linkage it is tried to one dimension of situation dimensions be chosen and considering the amount of φ_{ij} and moving toward or against it.

• Worker bees present their information about the situations of food sources to onlooker bees in dance floor, and then onlookers choose one of which according to the (2) formula:

$$p_i = \frac{fit_i}{\sum_{n=1}^{SN} fit_n} \text{ .....(2)}$$

In the above formula, fit_i is the amount of source's fitness for i_{th}bee. For the purpose of maintaining diversity we use sharing function instead of (2) which we will explain in the next section.

According to the (1), onlooker bees search a food source next to the chosen source in the previous step.If a source runs out of nectar, worker bee leaves the source and turns into a scout and begins to search a new source accidentally, that is, we are in an optimized local so the place is omitted and a new one is produced accidentally.

Each cycle of search includes three steps: movement of workers and onlookers toward the sources and calculating their fitness (their nectar) and determining the scouts and their random movement toward the possible sources.

A food source is a possible solution for a problem and the amount of source's nectar related to the quality of the solution. In this method onlookers choose more proportionate sources by a selection mechanism and at the end of each cycle scouts are chosen for random search and without any previous knowledge. Although these bees have low quality and expenditure, sometimes they can find unknown rich sources. But it is possible that each cycle has no scout, since we should determine sources (workers) which have not improved in algorithm of several cycles and replace them by producing accidental new sources. The number of cycles in which solution has not improved is determined by the limit variable. This amount is calculated by (3):

$$limit = SN * D(3)$$

SNis the number of bees and D is the dimension of problem.

A. Sharing Function Model

In this model [8] of creating diversity, the emphasis is on the decreasing the fitness of similar answers. If in each generation optimized answer is more than expected amount, it will be against the other optimized one. Therefore, the fitness of each agent answers should decrease. On the other hand, optimized answers which have lesser agents should be emphasized by selection performer. A population with the yield of f is commensurate with the number of answers of m. If there are q optimized answers, this concept shows that the proportion of yield f (the amount of target function) to m (the number of sub-populations) per each optimized answer should be the same:

$$\frac{f_1}{m_1} = \frac{f_2}{m_2} = \cdots = \frac{f_q}{m_q} \text{ .....(4)}$$

If the selection is commensurate with the amounts of sharing fitness, all the optimized answers are copied as the same expected amounts and as a result, similar emphasis will be on the optimized answers. For determining the number of answers for each optimized answer in this model, estimation function is used according to (6);

$$sh(d) = \begin{cases} 1 - \left(\frac{d}{\sigma_{share}}\right) if d \le \sigma_{share} \\ zero otherwize \end{cases} \text{ .....(5)}$$

d is the distance between two answers in the population. Above function is calculated regarding the amounts of d and σ_{share} on the range of [0, 1]. In a population an answer may impress by no sharing of any other answers or may receive any trivial impact of other sharing answers or may impress by itself. If the amounts of sharing function are added up, which are calculated by considering all of the population's members (including themselves), the situation number of nc_i for the i_{th} answer is calculated according to the (6):

$$nc_i = \sum_{j=1}^{N} sh(d_{ij}) \text{.....(6)}$$

Then this situation number is a calculation of amount of pooling around an answer. Here d_{ij} is the

distance between i_{th} and j_{th} answer. Ultimately, the amount of sharing's fitness namely, $f_i' = f_i/nc_i$ should be calculated. As all of the optimized answers that are greater than the agent have greaternc_i, the fitness of all their answers' agents should decrease significantly. All the optimized answers below the agent have the lesser amount of nc_i .Therefore we should not decrease their answers' fitness significantly,and accordingly more emphasis will be on the optimized answers below the agent.

B. Guardian Bees

In the version presented by Shayganpur[9], the sharing function model is set in algorithm for the purpose of preventing the convergence of answers. In such an algorithm when a worker bee endeavors as much as the number of variables in order to improve its position but fails to do so, it is the situation in which the bee is in a local optimize and turns into a scout and keeps on the random search in the place. So there is no process that guarantees the avoidance of repeated searching. On the other hand, in the environments which act repetitively there is probability that optimized points lie in places where they have been before. Nonetheless, there is no way to return to the previous peak.

```
Initialize population
Evaluate the population
Cycle = 1
Repeat
   if environment changed
      evaluate fitness of guardians
foreach guardians
        if fitness of guardian changed and guardian was
in valley
              discard it
elseif fitness of guardian changed and guardian wasn't
in valley
              keep it and add it as scout
endif
endfor
endif
foreach employed bees
      produce new solutions and evaluate them
      Apply greedy selection process
endfor
   use sharing function model and proportionate
selection
   produce new solution v_{i,j} for onlooker from the
solution x_{i,j} check not exist in guardians
   Apply greedy selection process
Determine the abandoned solution for scouts and add to
      vally_guardians andreplace it with new scouts
   Memorize best solution achieved so far and add to
peak_guardians
   Cycle = Cycle + 1
Until Cycle = MCN
```

Figure 1. pseudo-code of improved algorithm.

To do the above mentioned tasks we have used guardian bees. Guardian bees are divided into two groups: peak-guardians and valley-guardians. As their name imply peak-guardians protect peaks and valley-guardians protect local optimum in order to avoid retuning to those places. After a peak is discovered, a peak-guardian bee will be responsible for its protection in order to prevent repeated searching after some environmental changes. We suppose the list of the peak-guardian bees as a line which its length is a coefficient of numbers of peaks. Omission of guardians is done from the end of the line and with the emersion of a peak, its guardian stands at the start point of the line. After a change in a dynamic environment, the fitness of valley-guardians is evaluated and if it changes, the bee is exempted from guarding in that place. The pseudo-code of improved algorithm is depicted in the Figure 1.

IV. EXPERIMENTS AND RESULTS

For experiments the moving peaks benchmark function is used. The adjustments of this function are shown in Table1.

TABLE I. ADJUSTMENT OF MOVING PEAK FUNCTION

Parameters	Presupposed amount
Heightseverity	7.0
Width severity	1.0
The form of peaks	Cone
length of change (S)	1.0
λ	0
Number of dimensions	5
Minimum and maximum height	[30.0, 70.0]
Minimum and maximum width	[1, 12]
The range of search	[0, 100]

We have redone experiments with 10 to 50 peaks and in 10, 200, 500, 1000, 2500, 5000, and 10000 frequencies and the results of which have been shown in 2-6 Pictures. The scale of comparison is offline-error.

CONCLUSION

In this essay by adding elements named guardian bees to the algorithm of artificial bees based on the sharing function, an algorithm was presented which while improves the efficiency, shows acceptable performance in dynamic environments. Adding guardian bees impacts the efficiency of improvement in two ways: first maintaining so far found points for returning and the next is preventing from repeated searching in those places and have been left as local optimize. Considering carried out experiments, almost in all conditions the algorithm shows better performance in comparison to its original version. Multi-population algorithms are suggested with respect to its higher efficiency. This algorithm for local searching uses throngs around the examining points instead of using the population members.

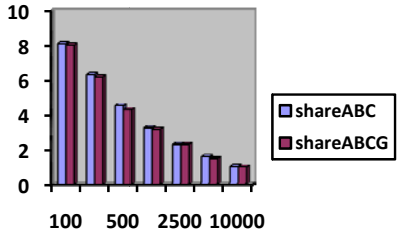

Figure 2. Compare offline Error in Environment with 10 peak.

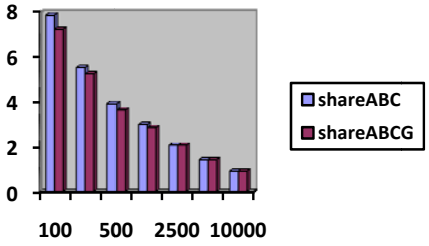

Figure 3. Compare offline Error in Environment with 20 peak.

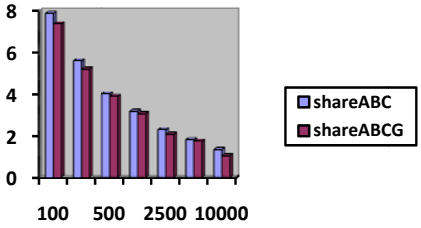

Figure 4. Compare offline Error in Environment with 30 peak.

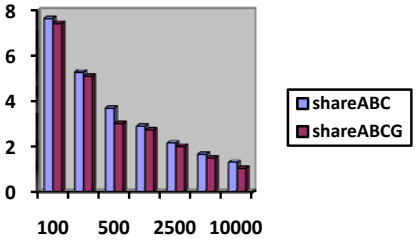

Figure 5. Compare offline Error in Environment with 40 peak.

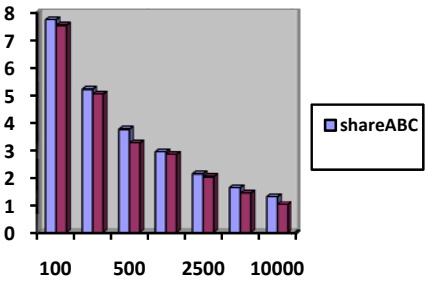

Figure 6. Compare offline Error in Environment with 50 peak.

Figure 7.

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COMPARATIVE STUDY OF DATA MINING TECHNIQUES FOR IMAGE CLASSIFICATION

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Abstract- Image classification plays an essential role in perception, reasoning, action, and goal-oriented behaviors. Over the past decades, this problem has attracted much attention in the machine intelligence. Image classification is perhaps the most important part of digital image analysis. The intent of the image classification process is to categorize all pixels in a digital image into one of several classes. I have studied different classification techniques and their comparison. This study presents most commonly used image classification techniques such as Decision tree, Bayesian classification, neural network, and Support vector machine.

Keywords: Bayesian, classification technique, support vector, Neural Network .

I. INTRODUCTION

Machine learning focuses on classification, based on *known* properties learned from the training data. There are several applications for Machine Learning (ML),the most significant of which is data mining. People are often prone to making mistakes during analyses or, possibly, when trying to establish relationships between multiple features. This makes it difficult for them to find solutions to certain problems. Machine learning can often be successfully applied to these problems, improving the efficiency of systems and the designs of machines. Machine learning is a type of artificial intelligence that provides computers with the ability to learn without being explicitly programmed. Machine learning focuses on the development of computer programs that can teach themselves to grow and change when exposed to new data. Classification in machine learning is a form of data analysis that can be used to extract models describing important data classes. Such analysis can help provide us with a better understanding of the data at large. Classification predicts categorical (discrete, unordered) labels.

Classification is a data mining (machine learning) technique used to predict group membership for data instances. He presented the basic classification techniques[10]. Bayesian-based probabilistic and information-theoretic search versus Prof. Alka khade classification decision-making criteria that result in guaranteed detection and classification[3][7]. A Support Vector Machine techniques is described with its advantages and disadvantages[7][5]. Neural Network ,its different types with its implementation, application is presented by Jeff Heaton[9].and Decision tree concept is introduced by J. R. Quinlan[1].

Image Classification process:

Image classification , A classifier is an algorithm that takes a set of parameters or features that characterizes Objects and uses them to determine class or type of Each object. Data classification is a two-step process.

1.Training Phase:

In the first step, a classifier is built describing a predetermined set of data classes or concepts. This is the learning step (or training phase), where a classification algorithm builds the classifier by analyzing or "learning from" a training set made up of database tuples and their associated class labels. Because the class label of each training tuple is provided, this step is also known as supervised learning. It contrasts with unsupervised learning (or clustering), in which the class label of each training tuple is not known, and the number or set of classes to be learned may not be known in advance. These processes can include statistical models, mathematical algorithm and machine learning methods.

Given a set of input items, X = {x1, x2, ... xn} and a set of labels/classes, Y = {y1, y2, ... yn} and training data T = { (xi, yi) | yi is the label/class for xi }, a classifier is a mapping from X to Y, f(T, x) = y

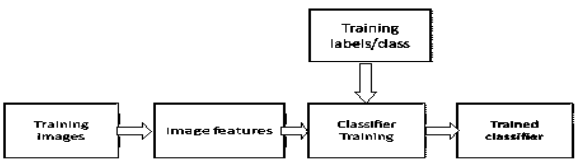

Figure 1: Training phase

2. Testing Phase:

Apply f to a never before seen test example **x** and output the predicted value y = f(**x**).

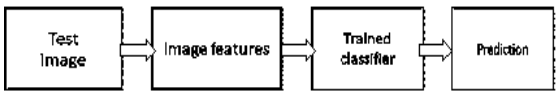

Figure 2: Testing phase

These process can include statistical models, mathematical algorithm and machine learning methods. In the present paper, we have concentrated on the techniques necessary to do this. In particular, this work is concerned with classification problems in which the output of instances admits only discrete, unordered values. Our next section presented different classification techniques as decision tree classifiers, Bayesian classifiers, Bayesian belief networks, and, k-nearest-neighbor classifiers, , Backpropagation (a neural network technique) is also discussed. in addition to a more recent approach to classification known as support vector machines. Classification have numerous applications, including fraud detection, target marketing, performance prediction, manufacturing, and medical diagnosis.

Preprocessing of the data in preparation for classification can involve data cleaning to reduce noise or handle missing values, relevance analysis to remove irrelevant or redundant attributes, and data transformation, such as generalizing the data to higher-level concepts or normalizing the data. Predictive accuracy, computational speed, robustness, scalability, and interpretability are criteria for the evaluation of classification and prediction methods.

This paper is organized as follows: In section II we discuss about the Decision tree technique of machine learning. we studied Bayesian classification in section III. Back propagation classification learning method described in section IV. In section V the recent technique Support Vector machine are discussed. Section VI presents the comparison on various machine-learning techniques and conclusions and future direction are presented in section VII.

II. DECISION TREE CLASSIFIER

Decision tree induction is the learning of decision trees from class-labeled training tuples. A decision tree is a flowchart-like tree structure, where each internal node (non leaf node) denotes a test on an attribute, each branch represents an outcome of the test, and each leaf node (or terminal node) holds a class label. The topmost node in a tree is the root node. How are decision trees used for classification?" Given a tuple, ***X***, for which the associated class label is unknown, the attribute values of the tuple are tested against the decision tree. A path is traced from the root to a leaf node, which holds the class prediction for that tuple. Decision trees can easily be converted to classification rules. Decision trees are constructed in a top-down recursive divide-and-conquer manner. The training set is recursively partitioned into smaller subsets as the tree is being built.

The algorithm, summarized as follows.
1. create a node N;
2. if samples are all of the same class, C then
3. return N as a leaf node labeled with the class C;
4. if attribute-list is empty then
5. return N as a leaf node labeled with the most common class in samples;
6. select test-attribute, the attribute among attribute-list with the highest information gain;
7. label node N with test-attribute;
8. for each known value ai of test-attribute
9. grow a branch from node N for the condition test-attribute= ai;
10. let si be the set of samples for which test-attribute= ai;
11. if si is empty then
12. attach a leaf labeled with the most common class in samples;
13. else attach the node returned by Generate_decision_tree(si,attribute-list_test-attribute)

During tree construction, attribute selection measures are used to select the attribute that best partitions the tuples into distinct classes. When decision trees are built, many of the branches may reflect noise or outliers in the training data. Tree pruning attempts to identify and remove such branches, with the goal of improving classification accuracy on unseen data.

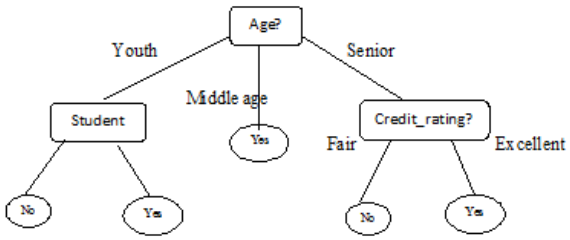

Figure 3: Decision tree

III. BAYESIAN CLASSIFICATION

Bayesian classifiers are statistical classifiers. They can predict class membership probabilities, such as the probability that a given tuple belongs to a particular class. Naïve Bayesian classifiers assume that the effect of an attribute value on a given class is independent of the values of the other attributes. This assumption is called class conditional independence. It is made to

simplify the computations involved and, in this sense, is considered "naïve." Bayesian classification is based on Bayes' theorem.

Bayes' Theorem:

Bayesian reasoning is applied to decision making and inferential statistics that deals with probability inference. It is used the knowledge of prior events to predict future events .Let ***X*** be a data tuple. In Bayesian terms, ***X*** is considered "evidence." As usual, it is described by measurements made on a set of *n* attributes. Let *H* be some hypothesis, such as that the data tuple ***X*** belongs to a specified class *C*. For classification problems, we want to determine *P*(*H*j***X***), the probability that the hypothesis *H* holds given the "evidence" or observed data tuple ***X***. In other words, we are looking for the probability that tuple ***X*** belongs to class *C*, given that we know the attribute description of ***X***. *P*(*H*j***X***) is the posterior probability, or *a* posteriori probability, of *H* conditioned on ***X***.

$$P(H|\boldsymbol{X}) = \frac{P(\boldsymbol{X}|H)P(H)}{P(\boldsymbol{X})}$$

Naïve Bays classifier:

It is based on the Bayesian theorem It is particularly suited when the dimensionality of the inputs is high. Parameter estimation for naive Bayes models uses the method of maximum likelihood. In spite over-simplified assumptions, it often performs better in many complex real world situations

Derivation:

1) D: Set of tuples

Each Tuple is an 'n' dimensional attribute vector

X : (x1,x2,x3,…. xn)

2) Let there be 'm' Classes : C1,C2,C3…Cm

Naïve Bayes classifier predicts X belongs to Class Ci iff

P (Ci/X) > P(Cj/X) for 1<= j <= m , j <> i

3) Maximum Posteriori Hypothesis

P(Ci/X) = P(X/Ci) P(Ci) / P(X)

Maximize P(X/Ci) P(Ci) as P(X) is constant

Naïve Assumption of "class conditional independence".

$$P(X/Ci) = \prod_{k=1}^{n} p\left(\frac{xk}{Ci}\right)$$

P(X/Ci) = P(x1/Ci) * P(x2/Ci) *…* P(xn/ Ci)

IV. CLASSIFICATION BY BACK PROPAGATION

A Neural network is a set of connected input/output units in which each connection has a weight associated with it. During the learning phase, the network learns by adjusting the weights so as to be able to predict the correct class label of the input tuples.

A Multilayer Feed-Forward Neural Network:

The back propagation algorithm performs learning on a multilayer feed-forward neural network. It iteratively learns a set of weights for prediction of the class label of tuples. A multilayer feed-forward neural network consists of an input layer, one or more hidden layers, and an output layer. Each layer is made up of units. The inputs to the network correspond to the attributes measured for each training tuple. The inputs are fed simultaneously into the units making up the input layer. These inputs pass through the input layer and are then weighted and fed simultaneously to a second layer of "neuron like" units, known as a hidden layer. The outputs of the hidden layer units can be input to another hidden layer, and so on. The number of hidden layers is arbitrary, although in practice, usually only one is used. The weighted outputs of the last hidden layer are input to units making up the output layer, which emits the network's prediction for given tuples.

Input layer Hidden Layer Output Layer

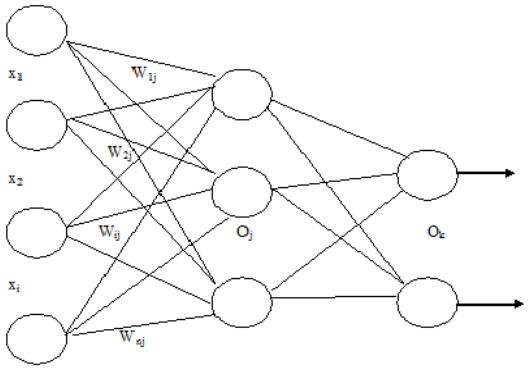

Figure 4: Multilayer feed forward network

Before starting training , the user must decide the number of input layer, number of output layer and number of hidden layer. We generally normalize the input values for each attribute between 0.0 to 1.0 to speed up the process. There are no clear rule to find number of hidden layer. It is a trial and error process so affect the accuracy of the system.

Backpropagation:

Backpropagation learns by iteratively processing a data set of training tuples, comparing the network's prediction for each tuple with the actual known *target* value. The target value may be the known class label of the training tuple (for classification problems) or a continuous value (for prediction). For each training tuple, the weights are modified so as to minimize the mean squared error between the network's prediction and the actual target value. These modifications are

made in the "backwards" direction, that is, from the output layer, through each hidden layer down to the first hidden layer (hence the name *backpropagation.*

Algorithm:
Backpropagation: Neural network learning for classification or prediction, using the backpropagation algorithm.

Input:
D, a data set consisting of the training tuples and their associated target values;
1. *l*, the learning rate;
2. network, a multilayer feed-forward network.

Output: A trained neural network.

Method:
(1) Initialize all weights and biases in *network*;
(2) while terminating condition is not satisfied {
(3) for each training tuple ***X*** in *D* {
(4) // Propagate the inputs forward:
(5) for each input layer unit *j* {
(6) $Oj = Ij$; // output of an input unit is Its actual input value.
(7) for each hidden or output layer unit *j* {
(8) $Ij = \sum_I w_{ij} Oi + \theta j$; //compute the net input of unit *j* with respect to the previous layer, *i*
(9) $Oj = \frac{1}{1+e^{-I}j}$; } // compute the output of each unit *j*
(10) // Back propagate the errors:
(11) for each unit *j* in the output layer
(12) $Err\,j = Oj(1-Oj)(Tj - Oj)$; // compute The error.
(13) for each unit *j* in the hidden layers, from the last to the first hidden layer
(14) $Err\,j = Oj(1-Oj)\sum_k Err_k w_{jk}$; // compute the error with respect to the next higher layer, *k*
(15) for each weight *wi j* in *network* {
(16) $\Delta w_{ij} = (l)\, Err\,j\, Oi$; // weight increment
(17) $wi\,j = wi\,j + \Delta wi\,j$; g// weight update
(18) for each bias θj in *network* }
(19) $\Delta\theta j = (l) Err\,j$; // bias increment
(20) $\theta j = \theta j + \Delta\theta j$; // bias update
(21) }}

V. SUPPORT VECTOR MACHINES

In this section, we study Support Vector Machines, a new method for the classification of both linear and nonlinear data. A support vector machine (or SVM) is an algorithm that works as follows. It uses a nonlinear mapping to transform the original training data into a higher dimension. Within this new dimension, it searches for the linear optimal separating hyper plane (that is, a "decision boundary" separating the tuples of one class from another). With an appropriate nonlinear mapping to a sufficiently high dimension, data from two classes can always be separated by a hyper plane. The SVM finds this hyper plane using support vectors ("essential" training tuples) and margins (defined by the support vectors).

The Case When the Data Are Linearly Separable:
let's consider an example based on two input attributes, *A*1 and *A*2, as shown in figure. From the graph, we see that the 2-D data are linearly separable (or "linear," for short) because a straight line can be drawn to separate all of the tuples of class+1 from all of the tuples of class-1. There are an infinite number of separating lines that could be drawn. We want to find the "best" one, that is, one that (we hope) will have the minimum classification error on previously unseen tuples. An SVM approaches this problem by searching for the maximum marginal hyperplane.
Consider Figure below which shows possible separating hyperplanes and

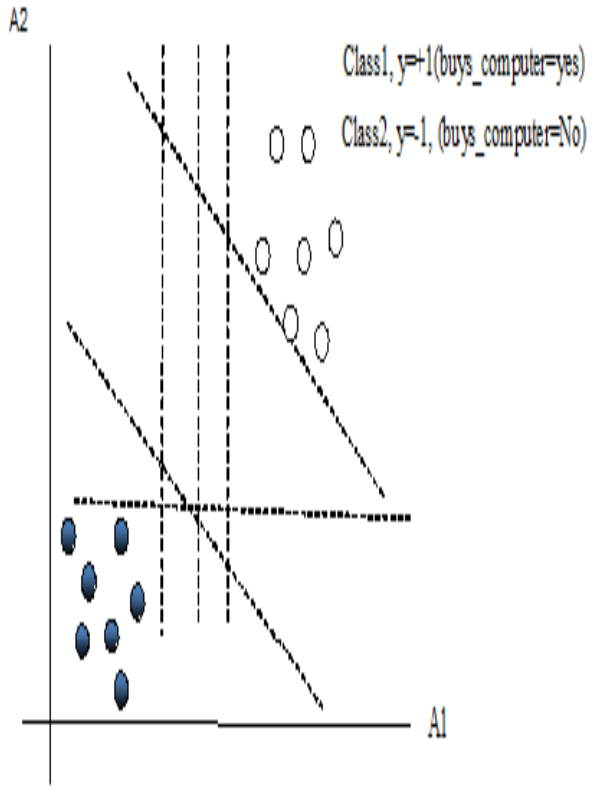

Figure 5 : The 2-D training data are linearly separable. There are an infinite number of (possible) separating hyper planes or "decision boundaries."

their associated margins. Intuitively, however, we expect the hyper plane with the larger margin to be more accurate at classifying future data tuples than the

hyper plane with the smaller margin. the SVM searches for the hyper plane with the largest margin, that is, the maximum marginal hyper plane (MMH). The associated margin gives the largest separation between classes. A separating hype rplane can be written as

$$\boldsymbol{W}.\boldsymbol{X}+b = 0;$$

Where $\boldsymbol{W}$ is a weight vector, namely W = ($w1$, $w2$, : : : , wn); n is the number of attributes; and b is a scalar, often referred to as a bias;

The Case When the Data Are Linearly Inseparable:
SVMs are capable of finding nonlinear decision boundaries (i.e., nonlinear hyper surfaces) in input space. We obtain a nonlinear SVM by extending the approach for linear SVMs as follows. There are two main steps In the first step, we transform the original input data into a higher dimensional space using a nonlinear mapping.. Once the data have been transformed into the new higher space, the second step searches for a linear separating hyper plane in the new space .We again end up with a quadratic optimization problem that can be solved using the linear SVM formulation. The maximal marginal hyper plane found in the new space corresponds to a nonlinear separating hyper surface in the original space.
It so happens that in solving the quadratic optimization problem of the linear SVM(i.e., when searching for a linear SVM in the new higher dimensional space), the training tuples appear only in the form of dot products, □(***Xi***).□(***Xj***), where f(***X***) is simply the nonlinear mapping function applied to transform the training tuples. Instead of computing the dot product on the transformed data tuples, it turns out that it is mathematically equivalent to instead apply a *kernel function*, $K(\boldsymbol{Xi}, \boldsymbol{Xj})$, to the original input data. That is,

$$K(\boldsymbol{Xi}, \boldsymbol{Xj}) = \square(\boldsymbol{Xi}) \,.\, \square(\boldsymbol{Xj}).$$

In other words, everywhere that □(***Xi***) .□(***Xj***) appears in the training algorithm, we can replace it with $K(\boldsymbol{Xi};\boldsymbol{Xj})$. In this way, all calculations are made in the original input space, which is of potentially much lower dimensionality! After applying this trick, we can then proceed to find a maximal separating hyper plane. The procedure is similar to that described in above linear method although it involves placing a user-specified upper bound, C, on the Lagrange multipliers, ai. This upper bound is best determined experimentally

CONCLUSION

The main Contribution of this paper is to study different machine learning technique with respect to Image classification. The paper also gives a relative comparison of all the techniques based on their accuracy, speed, applications, advantages and limitations. After analysis of all the techniques, we cannot state as any one technique being the best. Each technique has different application areas and is useful in different domains based on its advantages. Thus, keeping in mind the limitations of each of the techniques and also the prime focus being the improvement in performance and efficiency we should use that technique, which best suits a particular application. Our study also encourages that no one technique can be classified as being the perfect machine learning technique. For this reason there is a strong need for better insight into the validity and generality of many of the discussed techniques.

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COMPARISON OF CLASSIFICATION TECHNIQUES

Table 1: Comparison of Image Classification Techniques

Method Name	**Decision tree**	**Bayesian classification**	**Backpropagation: Neural network**	**Support vector machine**
Key points	Simple and Fast, Easy to understand	Fast, good performance as compare to decision tree and neural network.	High tolerance of Noisy data, Very fast	very less over fitting problem as compared to other method.
Accuracy	Good Accuracy	High accuracy	Good accuracy	Very highly accurate
Error Rate	Moderate error rate	Minimum error rate compared all other classifiers	Ability to classify patterns that are not trained.	minimum compared to decision tree .
Learning used	Best for discrete-valued,	a quantitative approach	for learning real-valued, discrete-valued, and vector-valued functions	For linear and non linear data
Parameters for learning algorithm	the splitting criterion, pruning options, and smoothing (Laplacian or Bayesian smoothing), Tree models used are C4, ID3, CART.	Weka options for handling continuous attributes as modeling them as a single normal,	train neural nets with gradient descent back prop and vary the number of hidden units as 1,2,4,8,32,128.	Use the following kernels as Sigmoid kernel, polynomial kernel of degree 2 & 3,
Application areas	Medicine, Manufacturing, Products, Financial analysis.	Classify text documents, shape of object, Gender classification.	Handwritten character recognition, pathology Testing Effort Estimation Function Point Analysis, Risk Management, Reliability Metrics, Sales Forecasting	Handwritten digit recognition, object recognition, Speaker identification, Benchmark time series prediction tests.
Limitation	Over fitting the training data, poor predictability of data.	Requires long training time, they typically require initial knowledge of many probabilities.	Minimizing over fitting requires a great deal of computational effort. Efficiency depends on the time spent on training the network. Long training times	Extremely slow method Of Classification

LOW POWER AND AREA EFFICIENCY OF SHA-1 AND SHA-2 HASH ALGORITHM

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Abstract—This paper summarizes about the design of a Low Power and Efficiency of SHA-1 and SHA-2 Hash Functions capable of performing all members of the Secure Hash Algorithm (SHA) group of Hash Functions. The need for high-speed cryptography is introduced, as well as the SHA-1 and SHA-2 Hash Functions and their operation. Work performed at other institutions to improve throughput and power consumption is presented with advantages and disadvantages discussed. The ASIC design is then discussed, with comparisons made to previously publish ASIC and FPGA implementations. The possibility of using this ASIC architecture for the SHA-3 candidates, as well as the Message Digest (MD) families of Hash Functions is suggested as an area of future work as it is shown the ASIC Architecture designed would be capable of this with only program modifications required.

Keywords : Cryptography, Hash Function, Secure Hash Algorithm

I. INTRODUCTION

The growth rate for e-commerce has been double-digit over the last decade, with an estimated $301 billion expected online retail sales in 2012. This extreme increase in online trading has lead to a rise in online attacks to obtain money through deception or other illegal means. Due to this, companies and consumers have become more aware of
Security risks exchanging information over such an open medium, leading to several third parties setting up secure areas for credit card and bank account details to be shared with
Minimal risk of the numbers being obtained and used fraudulently. Major credit companies such as Visa and MasterCard have set up subsidiaries such as Verified by Visa to give consumers confidence that the sites they are buying from are safe. These "security seals" are becoming more common on commercial sites, as customers have been found to avoid purchasing from companies who do not use them. When shopping on The Internet, a connection is set up between the computer being used and the company server using a "Challenge and Response" through the Transport Layer Security (TLS), or its predecessor Secure Sockets Layer (SSL). The typical operation for this can be seen in Fig 1, using hash functions at both the Client and Server end to ensure a connection is secure without the need for cryptographic key exchange. A connection is only accepted if
The received and calculated values of cr and sr match.

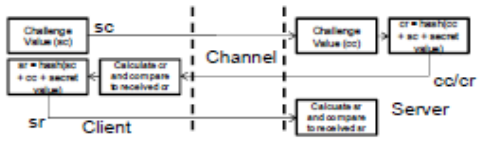

Fig 1. A typical Challenge and Response Scenario.

Secure Hash Algorithm (SHA) is the most widely used Hash Function in the world. It was developed by the National Institute of Standards and Technology (NIST) in the United States and first published in 1993. The original version (SHA- 0) was found to have a serious security flaw and replaced in 1995 with SHA-1.As computing power has increased, this too is found to have weaknesses and the possibility of collisions has been identified. To further enhance security, SHA-2 was released in 2001 containing improvements in the message computation and hash output size. To date, no weaknesses have been identified in SHA-2. Like all Hash Functions, SHA outputs a fixed length digest of a message with arbitrary input length. The original message is converted to blocks of a fixed size, which are sequentially reduced. This is repeated for the entire file, giving a message digest. Due to the Preimage resistance of SHA (the inability to find the
Message from the hash function), the method of operation can be made public. Would-be attackers gain no benefit from knowledge of the SHA Algorithm, as no key is used to create
the message digest. Both published variants of SHA work in a similar way, taking an arbitrary length input, sectioning this to 512-bit blocks (with padding where necessary to ensure the
message length is a multiple of 512) and processing these 512- bit blocks through rounds of addition, shifting and logical operations to produce a hash output of either 160 bits (SHA-1) or 224/256/384/512 bits (SHA-2) [6].

Although SHA-2 is increasing in popularity, SHA-1 is still significantly used, not least for its incorporation into the Trusted Platform Module (TPM) ASIC. However, TCG are currently investigating the use of SHA-2 in later module. If this takes place, the TPM ASIC will also have to contain backwards-compatibility to SHA-1 for communication with older modules. Therefore, it is

important that an ASIC can manage creation of SHA-1 and SHA-2 message digests at a speed where delay would not be noticed on a high-speed internet connection.

II. PREVIOUSLY PUBLISHED SHA-1 AND SHA-2 DESIGNS

Most published work regarding FPGA or ASIC implementation of SHA concentrates on either SHA-1 or SHA-2 with no work found on a fully integrated ASIC. Chaves proposes core layouts for both SHA-1 and 2, but does
not integrate these into a common core. The implementations found are also only capable of performing one hash function. Due to the high number of different hash functions available, a fully flexible implementation would be of great use, even if this flexibility comes with a throughput penalty.

A. Throughput Improvements

Zeghid and Wanzhong both identify reducing the critical path for calculation through the substitution of Carry Save Adders (CSA) for slower Carry Look-Ahead Adders (CLA). CSAs are capable of performing addition of three numbers, rather than the two that CLA or Full Adders (FA) can perform Xia, in however, uses Full Adders, placing them into a Wallace Tree to reduce the critical path.
Both methods show speed benefits, with giving a maximum throughput of 2073 Mbit/sec for SHA-256 and 950Mbit/sec for SHA-1 in [12] with throughput calculated
Using

$$\text{Throughput} = \frac{\text{Block size}}{\text{Clock period} + \text{Latency}}$$

The reduction in Critical Path for the longest calculation allows the remainder of the SHA operation to be unrolled and therefore completed in one, rather than multiple, clock cycles. It is found in that unfolding the design for two operations (so performing two operations in one clock cycle) gives a factor-of-two speed improvement for the same increase in area. Unfolding is also performed in [14], increasing throughput to 76Mbit/sec in conjunction with pipelining. Changing the architecture to a pipeline allows for simultaneous processing of blocks while not affecting the SHA operation. Using the pipeline also gives a level of delay balancing to the circuit, preventing incorrect signal
Propagation through a circuit and causing an incorrect message digest. Use of these improvement techniques comes at a gate penalty and therefore would not be ideal for
applications where power consumption is critical.

B. Power Consumption Improvements

Power Consumption is a key factor in all modern integrated circuit design. Due to the increase in wireless and mobile internet, systems are more commonly running from battery power rather than a mains supply. Therefore, reduction in both dynamic and static power consumption must be considered.
The main consumer of dynamic power is the clock signal, so reducing either its speed or proliferation through the circuit would have a noticeable effect. Reduction of the clock speed
is not recommended, as this will reduce the number of computations that can be performed per second and therefore the throughput of the circuit. Due to this, methods of reducing its presence in the circuit take priority. In both Locally Explicit and Bus Specific Clock Enabling are suggested as methods to reduce power. These take the clock signal and only
allow it to propagate into areas of the circuit when a signal is applied to the sub-sections input. By doing this, the number of transistors the clock is applied to is reduced and therefore the capacitance it must charge/discharge in a clock cycle, thus reducing the dynamic power consumed on each clock event. As

$$Dynamicpower = Frequency + Capacitency + Voltag^2$$

This technique is found to save up to 65% of the dynamic power, without altering any gate propagation times or overall operational speed.
Static power reduction is more difficult to implement, but equally important as leakage power loss can account for up to 50% of power consumed by an ASIC. Little work can be found on reducing this in cryptographic ASICs, but techniques such as Logic Gating could be used to deactivate areas when not in use. However this would mean any data in these areas has to be stored before deactivation, increasing the register count for the ASIC. Due to the time constraints of the project, reductions in static power were not investigated further. A final method for increasing throughput suggested in and tested in [18] is the use of Very Long Instruction Word (VLIW) to increase parallelism. These papers suggest that having multiple sets of instruction commands to set logic prior to data arriving would improve throughput. Qualitative improvements for this have been noted and this was deemed aviable extension item to the base ASIC design.

III. PROJECT GOALS AND DESIGN

A. Goals

This project lead to the design of ASIC containing functional blocks for performing SHA-1 and SHA-2. This design was intended to be flexible, allowing other Hash Functions to be executed through changing the program within the ROM. Due to time constraints, this chip was not physically

manufactured; instead it was simulated and run using a constructed test bench in VHDL. Since VHDL is standardized by the IEEE, it was felt to be more suitable for use than other languages such as Verilog. For these simulations, timing
Considerations were not taken into account.

B. Design

To allow a design capable of performing all variants of the SHA family, a modular approach to the design was taken. This can be seen in Fig 2. The ASIC has one common 32-bit bus, allowing movement of data between sections of the architecture based on the command extracted from ROM and interpreted at the Instruction Register. Differences between SHA-1 and 2 such as the value of initialization vectors are stored in ROM and extracted by requesting their memory address within the program. The ASIC uses tri-state buffers to store data, reducing read/write operations to RAM and eliminating the need for a cache, as well as ensuring the bus can be shared by all components without corruption through the use of their high impedance state.
The ASIC has 36 data pins; with 32 connected to the I/O block, plus a clock pin, a "more message" pin, a selector for SHA-1 or SHA-2 and an asynchronous reset. The reset will place the FSM back into its initial state whenever it is set, as well as clear all register and RAM content. Initialization Values (IV's) and calculation constants (K) will not be affected by the reset, as these are stored in ROM.

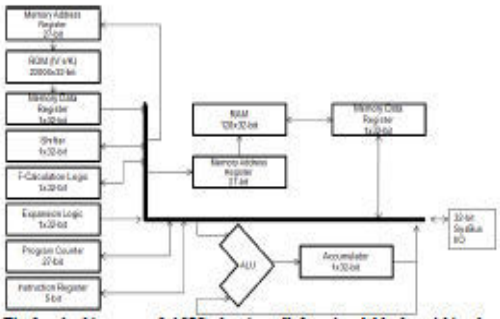

Fig 2. Architecture of ASIC showing all functional blocks within the ASIC connected by a common 32-bit bus

1) Execution of Programs

The program to execute the hash function in stored in ROM and called by incrementing the Program Counter (PC). This is a 27-bit binary counter, incremented by setting an increment
flag. The PC may also be reset to allow repeated looping of the program for messages larger than 512-bits, or jumped to a value stored in ROM to allow different programs to be executed. This allows multiple programs to be stored in ROM, such as SHA-1, variants of SHA-2 or Message Digest (MD) hash functions, giving the ASIC a great deal of flexibility. The program stored in ROM consists of a 32-bit number containing an 18-bit operations code (opcode) and 14-bit RAM address for this to be executed upon. To allow execution of SHA-1 and 2, approximately 22000 lines of code were required, with another 81 locations in ROM required from
Initialization vectors and constants. The opcode is decoded by the Instruction Register and are broadly split into four types; load; store; pass and execute. Load commands place a value from the specified RAM address into a block's tri-state registers. Store commands take the value stored in a specific blocks tri-state registers and place it at the address specified in RAM. Pass allows movement between tri-state registers of different blocks without the use of RAM to increase throughput. The execute command will run a logic block and update its tri-state register with the new result. To execute an opcode, a fetch section increments the program counter and
loads the relevant command from ROM into RAM. This is then placed in the instruction register, which splits the 32-bit value received into the Opcode and the RAM address to be
extracted (if required). The Opcode is then set within the ASIC, allowing progression through the controlling state machine. Each Opcode takes between 50 and 70us to execute, depending on its location within the state machine. All opcodes can be seen in Table I.

2) Arithmetic Logic Unit

The ALU in this case is a full adder that performs modulo- 32 additions on the value in its accumulator and the value on the bus. The result is stored in the accumulator for transfer to RAM or another functional block. The capability to perform full addition with a carry out is present in case a future hash function requires it, but unused at this time.

3) Shift Register

To perform the logical shifts present in SHA, a shift register was created. This allows parallel loading through the tri-state registers and will then run a set number of times depending on the opcode loaded. As an example, SHA-1 uses a 30-place left circular shift within its calculation. For this, an opcode was created that would run the shifter this number of times and allow other logical blocks to execute while this was taking place. Once the shift was complete, a completion flag is set, allowing the value in the tri-state register to be moved to another block when required.

4) Logic Calculation

SHA also uses a great deal of logical calculations within the message digest creation. For example, in

SHA-1 on rounds 40-59, the following logical sum is used

F= (b.c) + (b.d) + (c.d)

Where b, c, d and f are all 32-bit blocks of the 512-bit message. Initially, opcodes capable of performing all basic logic functions were created and these equations performed one factor at a time. To increase throughput, further opcodes were added to perform all aspects of SHA-1 and 2 by loading 32-bit blocks to multiple tri-states within the logic block and executing all items in an unrolled function. This gave a great increase in this blocks throughput for a small size penalty.

5) Memory Management

For accessing the ROM and RAM, two sets of registers were added. A Memory Address Register (MAR) and Memory Data Register (MDR). The MAR was used to access the address specified within the opcode and either place the data from this address into the MDR, or load data from the MDR into this address depending which opcode had been loaded into the instruction register. The use of MDR/MAR prevents memory directly writing to the bus and therefore minimizes the possibility of data corruption should the bus exhibit problems.

TABLE I
OPCODES IN ASIC AND USES WITHIN PROGRAM

Opcode	Use	Opcode	Use
Store ACC	Store Accumulator to MDR	Load ACC	Load Accumulator with MDR
Store Expansion	Store Expansion Logic to MDR	Load Expansion	Load Expansion Logic with MDR
Store Logic	Store Logic to MDR	Load Logic	Load Logic with MDR
Store Shifter	Store Shifter to MDR	Load Shifter	Load Shifter with MDR
Store ROM	Store Value In ROM to MDR	Left Shift	Runs Left Shift Operation
Logic Calculation1	Run AND Logic	Logic Calculation2	Run OR Logic
Logic Calculation3	Run NOT Logic	Logic Calculation4	Run XOR Logic
ALU Add	Performs Modular Addition	More Message	Denotes if message on input to Bus is complete
Message Out	Output Message to IO	Expansion Calculation	Runs Block Expansion
Store IO	Store IO to MDR	Load IO	Load IO with MDR
Shift2ALU	Load ALU with Shifter	ACC2Logic	Load Logic with Accumulator

IV. RESULTS

All components of the ASIC in Fig 2 were tested individually by simulation in VHDL using a set of instructions that gave a known output. The correct output from the blocks was placed into the ASIC through the "assert" statement to compare the outputted result and note any errors in the terminal window of the simulation software. All blocks within the ASIC performed as expected and were integrated into a complete system through the use of packages and component

Instantiation in VHDL. The test benches were designed to test all aspects of operation and feasible conditions of use to identify any issues in the modules [20]. Through this separate testing, some small coding errors were identified and corrected prior to their integration in to the main ASIC. Most errors

identified were omissions of commands such as setting the tristate register to high impedance when not requested to output to the bus. An omission such as this could cause the system bus to be used by two components simultaneously and therefore cause communication collisions. As no protocol to

Identify this (such as CDMA [21]) was implemented along with its associated error checking, any collisions could cause severe issues to the ASIC operation. Therefore, the correction of this code was critical to allowing successful operation of all modules within the system.

Once the SHA-1 ASIC was deemed to be operating successfully, the addition of SHA-2 to the core was made. Due to the modular design used, minimal additions needed to be

made to give this chip SHA-2 capabilities: A larger ROM was declared, to contain the extra IV and K values used by SHA-2 for its round calculations, along with the new program, and the addition of right linear and circular shifters to the shifter logic block

TABLE II
COMPARISON AGAINST PUBLISHED IMPLEMENTATIONS

Implementation	SHA Variant	Logic Blocks Used	Clock Frequency/ MHz	Throughput/ Mbit/sec
Kakarountas	SHA-1	950	98.7	2526.7
Sklavos	SHA-1	1004	42.9	119
Lee	SHA-1	2894	118	5900
Chaves	SHA-2	565	227	1420
Sklavos [22]	SHA-2	2384	74	291
Khalil [23]	SHA-2	4489	50	644
This Work	SHA-1	6836	100	162
This Work	SHA-2	6836	100	98

Note: The throughput values for this work are estimated based on all code-optimization and parallelism improvements identified being implemented.

Though the size of this work seems large compared to other published ASIC/FPGA implementations, this includes the ROM containing the program. If an external RAM/ROM is used, the size of this ASIC implementation decreases to 284, a factor of two lower than Chaves work in [8].

V. CONCLUSION

The ASIC within this paper allows for a reprogrammable design capable of performing the majority of common hash functions. Although only SHA-1 and 2 have been investigated initially, reprogramming the ROM would allow execution of other commonly used functions such as MD4/5. It is also possible for this ASIC to calculate some of the shortlisted SHA-3 algorithms, though the opcodes would not be optimized for these alternate functions. SHA-1 and 2 were chosen for optimization due to their widespread use and integration into the Trusted Platform Module. Therefore, the flexibility of running other hash functions would lead to a speed trade-off for this added ability. Through the use of VHDL, no limitations have been placed

on the manufacturing techniques that can be used to create this ASIC.. The architecture already has been successfully synthesized in Xilinx for the QPRO Vertex 4 FPGA, and could no-doubt be used on others also. Since most other work has been completed at the 0.13-0.18μm level, it is believed that this ASIC could also be built using these dimensions without major issues occurring.

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CONTROL AND SIMULATION OF INTEGTRATED PHOTOVOLTAIC CELL- BATTERY -FUEL CELL BASED DISTRIBUTED GENERATION SYSTEM FOR CONTROLLED AC LOADS

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Abstract— Utility restructuring, cutting-edge power electronics, public environmental concerns, and expanding power demand are providing the opportunity for emerging generation technologies in the modern world. In order to meet sustained load demands during varying natural conditions, different energy sources need to be integrated with each other for extended usage of alternative energy. The paper presents the modeling and control framework of a photovoltaic cell-battery-fuel cell(PVBFC) integrated stand-alone distributed generation system(DGS) in Matlab/Simulink environment. A new control strategy for charging and discharging controller(CDC) of generic battery(GB), maximum power point tracker(MPPT) for photovoltaic cell(PVC) and fuel flow rate controller(FRC) for fuel cell(FC) are developed. GB works in parallel with PVC to compensate varying natural conditions in day time and FC works independently at night. we also design an inverter model for the proposed system by considering the output voltage regulation.

Keywords-component: PVC, MPPT, PEMFC, GB, DGS, Voltage Regulation

I. INTRODUCTION

The conventional fuel energy sources such as petroleum, natural gas, and coal which meet most of the world's energy demand today are being depleted rapidly. Also, their combustion products are causing global problems such as the greenhouse effect and pollution which are posing great danger for our environment and eventually for the entire life on our planet **[**1**].** The alternative energy sources (PVC,FC,GB etc.) are attracting more attention. Today, new advances in power generation technologies and new environmental regulations encourage a significant increase of distributed energy resources(DER) around the world. DGS has mainly been used as a Stand-alone power system[2].

A detailed approach to PVC, FC and GB modeling based on a mathematical description of the equivalent electrical circuits are given in [3-4],[5] and [6] respectively.

Tracking the maximum power point(MPP) of a photovoltaic(PV) array is usually an essential part of a PV system. Much focus has been on hill climbing [7], and perturb and observe (P&O) methods[8,9]. Hill climbing

involves a perturbation in the duty ratio of the power converter, and P&O a perturbation in the operating voltage of the PV array.

The system under study in this paper is a stand-alone PVBFC integrated power system, which consists of a PVC, GB and a proton exchange membrane fuel cell(PEMFC). A simulation software program known as MATLAB/SIMULINK is used in dealing with modeling, simulation, control and energy management of the system under study. MPPT for PVC, CDC for GB and FRC for PEMFC are developed to get optimal system performance. The configuration of overall DGS system is a PVBFC integrated voltage source, a voltage source inverter (VSI) with a LC filter and two controlled AC loads.

II. MAIN COMPONENTS OF THE PROPOSED DGS

The basic components of the proposed DGS are DERs and their controllers, VSI with LC filter, and AC loads.

A. Modeling of DERs

The equivalent circuitry of a PV cell shown in Fig.1, the simplest model can be represented by a current source in parallel with a diode, and the non-idealities are represented by the insertion of the resistances Rs and Rp.

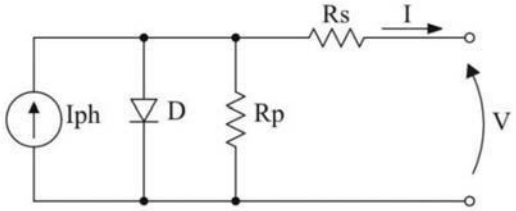

Fig.1: Equivalent Model of the Photovoltaic Panel.

$$I=I_{ph} - I_d - V_d/R_p \quad (1)$$

$$V= V_d - R_s * I_{\_pv} \quad (2)$$

$$I_d=I_{sat}*\exp(V_d/V_T -1) \quad (3)$$

$$V_T=k*T/q*Q_d*N_{cell}*N_{ser} \quad (4)$$

Where,

I_d = Diode cuurent (A)
V_d = Diode voltage (V)
R_s=Series resistance(Ω)
R_p=Shunt resistance(Ω)

I_{sat} = diode saturation current (A)
T = cell temperature (K),
V_T =temperature voltage(V)
k = Boltzman constant = 1.3806e-23 $J.K^{\wedge-1}$
q = electron charge = $1.6022e^{-19}$ C
Q_d = diode quality factor
N_{cell}= number of series-connected cells per module
N_{ser} = number of series-connected modules per string

B. Control Schemes for DERs

Hill climbing involves a perturbation in the duty ratio of the power converter, and P&O a perturbation in the operating voltage of the PV array. In the case of a PV array connected to a power converter, perturbing the duty ratio of power converter perturbs the PV array current and consequently perturbs the PV array voltage. A flow chart for MPPT algorithm is developed as shown in Fig.2.

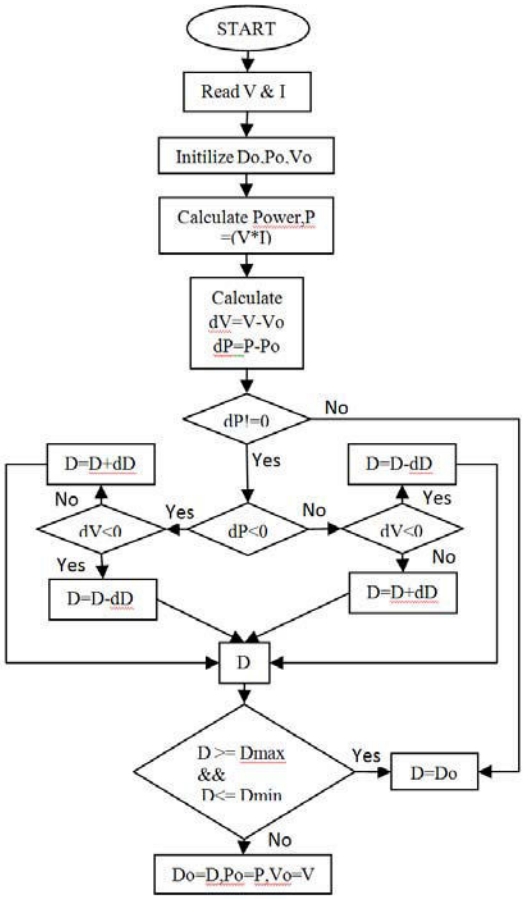

Fig. 2: Flow chart of MPPT Algorithm.

From Fig. 3, it can be seen that incrementing (decrementing) the voltage, increases (decreases) the power when operating on the left of the MPP and decreases (increases) the power when on the right of the MPP. Therefore, if there is an increase in power, the subsequent perturbation should be kept the same to reach the MPP and if there is a decrease in power, the perturbation should be reversed. The process is repeated periodically until the MPP

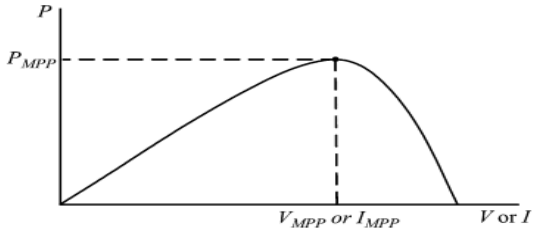

Fig.3: Maximum power point for PV Array .

is reached. The system then oscillates about the MPP. The oscillation can be minimized by reducing the perturbation step size.

The Power converter i.e the boost converter boosts DC voltage from V_{MMP} to 500V. This converter uses a MPPT system which automatically varies the duty cycle in order to generate the required voltage to extract maximum power.

Basic equation of boost converter is

$$Vo = \frac{1}{1-D} Vin \quad \ldots\ldots\ldots\ldots(5)$$

Where,

Vo=Output Voltage
Vin=Input voltage
D=duty cycle

The boost converter is designed in such a way that the Vo is again regulated to fixed voltage with the help of controlled voltage source converter of 500V.

A control algorithm shown in Fig.4 is developed for the CDC of the battery. The battery status signal i.e state of charge(SOC) is compared with upper and lower limit of SOC(%) in which limit battery works properly.

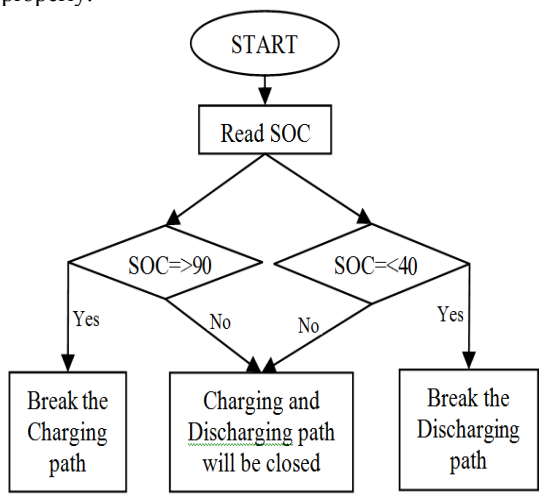

Fig.4: Flow chart for CDC of Battery.

A fuel cell current controlled fuel flow rate regulator is derived from [**5**]. The fuel flow rate is directly proportional to fuel cell current.

III. SIMULATION MODEL OF PVBFC SYSTEM

The models are integrated in Sim Power Systems(SPS) and used in a simulation of a PVBFC System. As shown in . Fig. 8 ,it consists of three DERs with their controllers, a IGBT voltage source inverter with PWM gate controller and two AC loads in which one is controlled. The four power(KW) displays show the status of power generated and observed by DERs and AC loads. subsystem block(light blue color) is opened to display additional scopes and measurements.

A: PWM IGBT inverter

A 3-phase 6-switch DC/AC PWM voltage source inverter is used to convert the power from DC to AC. Fig. 5 shows the main circuit of a 3-phase voltage source inverter, which is actually an IGBT-diode universal bridge.

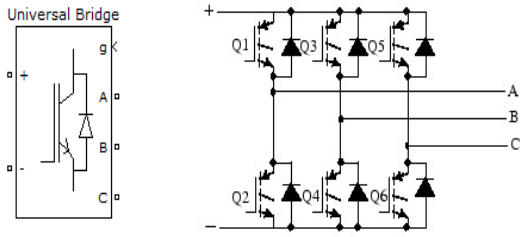

Fig. 5: IGBT-Diode Universal Bridge

This VSI needs gate pulses which is generated by PWM generator.

B: PWM Generator

The PWM Generator block generates pulses for carrier-based PWM converters using two-level topology. The block can be used to fire the forced-commutated devices (FETs, GTOs, or IGBTs) of single-phase, two-phase, three-phase, two-level bridges or a combination of two three-phase bridges.

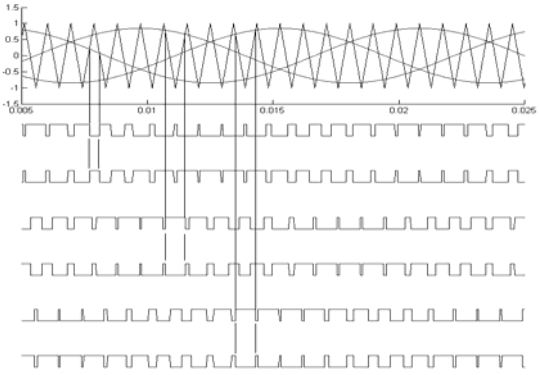

Fig. 6: Six pulses generated by the PWM Generator.

The pulses are generated by comparing a triangular carrier waveform to a reference modulating signal. The modulating signals can be generated by the PWM generator itself, or they can be a vector of external signals connected at the input of the block.

The modulation index(m) of modulated signal is externally controlled by voltage regulator block.

C: Voltage Regulator

The voltage regulator takes three components of load voltage in per unit(pu) as feedback, applies proper operation to control the modulation index.

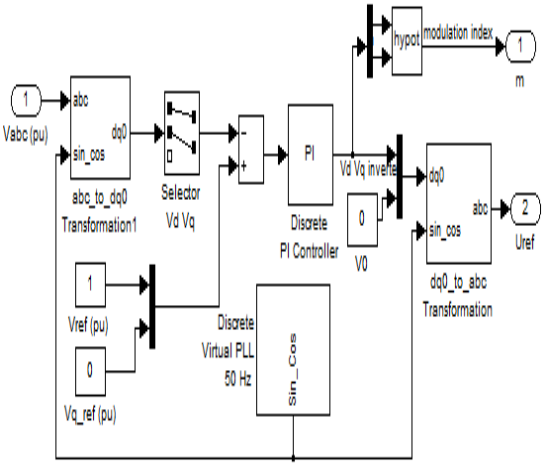

Fig.6: Simulated model of voltage regulator.

D: LC Filter

The primary function of the AC filter is to filter out the high frequency components caused by the inverter switching operation. The LC-filter aims to reduce the high order harmonics which are the multiples of the carrier frequency of PWM generator. The transfer function of the LC-filter designed by the output voltage to the input voltage is given as follows:

$$G(s) = \frac{1}{1 + LC\,s^2} \qquad (6)$$

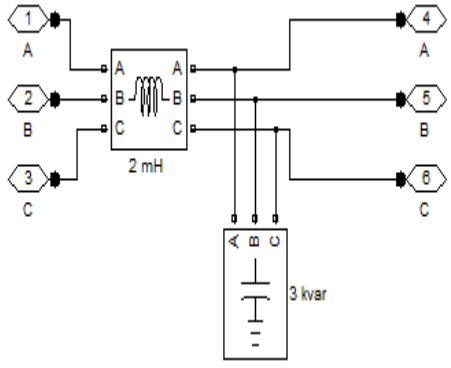

Fig. 7: Simulated model of LC filter.

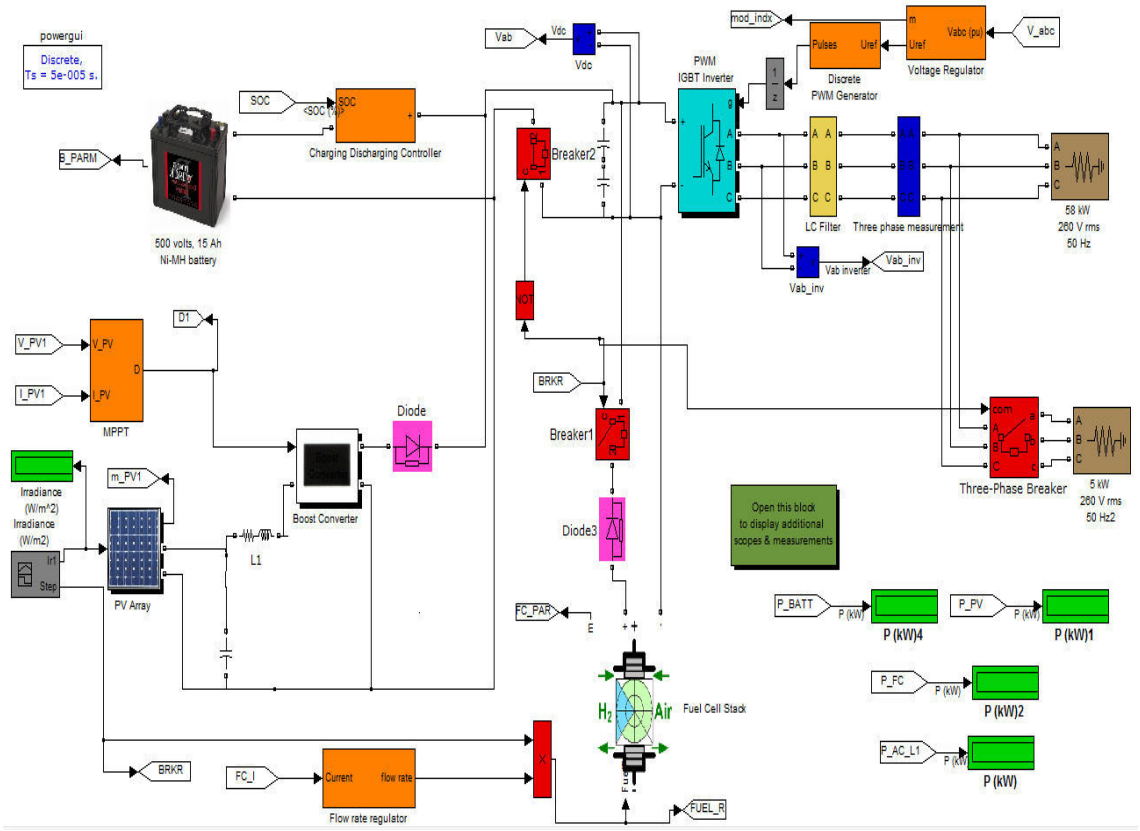

Fig. 8: Simulated model of PVBFC System

IV. SIMULATION PARAMETER OF COMPONENTS

Table I shows the parameter details of components in proposed PVBFC system.

Table I:

Name of Components	Details about the Component
PVC	Power=100KW , V_o=273.5V at 1000 W/M^2 Irradiance
PEMFC	Power=65KW,V_o=500V
GB	Rated Capacity=15Ah,V_o=500V
MPPT	Tracks Maximum Power Point and Varies duty cycle of Boost Converter
Boost Converter	Boost the V_{mpp} to fixed 500V
FRC	Regulates the fuel flow rate w.r.t fuel cell current
CDC	Control SOC in between 40% to 90%.
PWM IGBT VSI	Convert 500Volt(DC) to 280V(rms) (3-Phase AC)
PWM Generator	3 arm,6 pulse, carrier Frequency=2000KHz
Voltage Regulator	Regulates modulation Index to m=0.875 for PWM Generator
AC Load1	V_{rms}=260V,f=50Hz,Power=64kW
AC Load2	V_{rms}=260V,f=50Hz,Power=5kW

V. SIMULATION INPUT AND RESULTS

The PVBFC is simulated over 24s in which the first 12s, battery works in parallel with photovoltaic cell to compensate varying natural conditions in day time and fuel cell works independently at night for the next 12s. The varying natural condition is shown Fig. 9 from t=3s to t=5s. Fig. 10-15 show the simulation results.

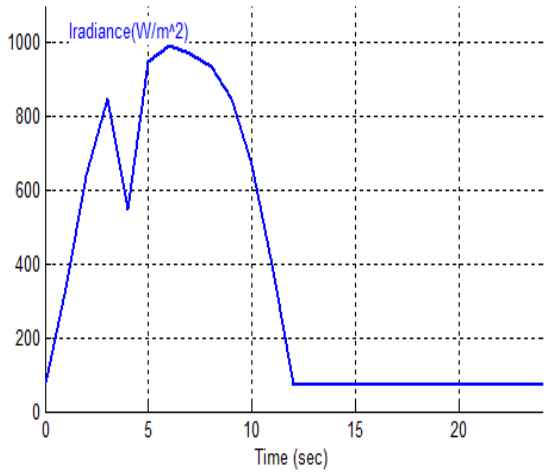

Fig.9: Irradiance versus Time signal with varying natural condition.

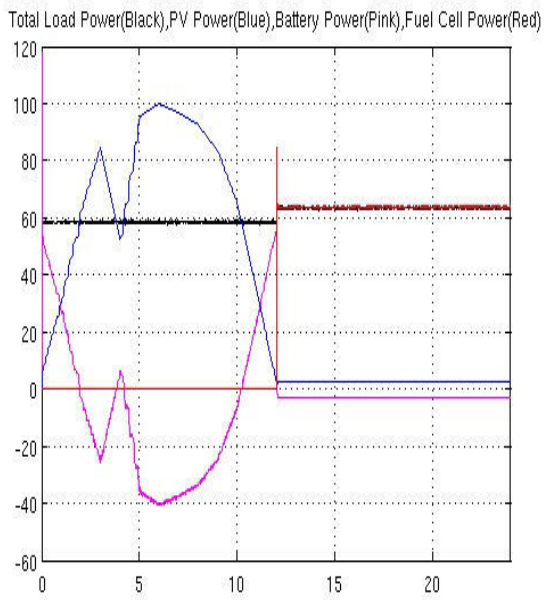

Fig.10: Power(KW) graph.

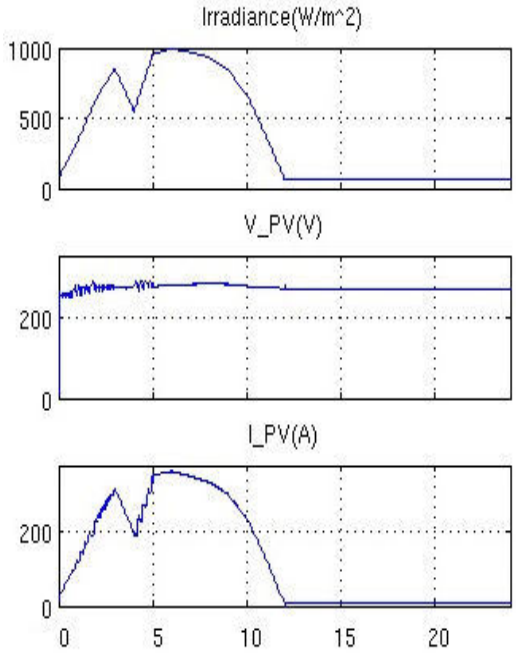

Fig.11: PVC status.

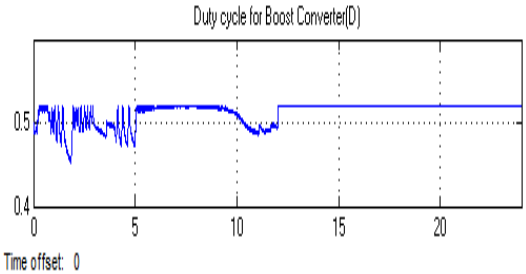

Fig. 12: Duty cycle variation of boost converter.

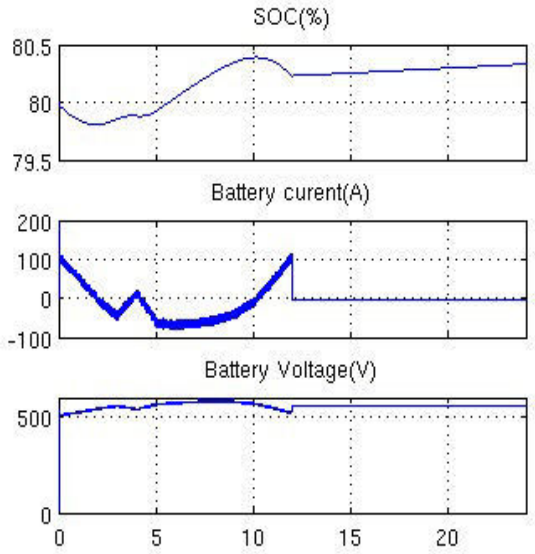

Fig.13: Battery status.

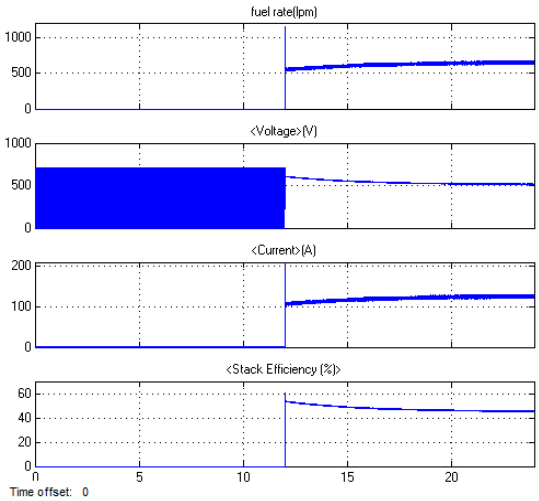

Fig.14: PEMFC status.

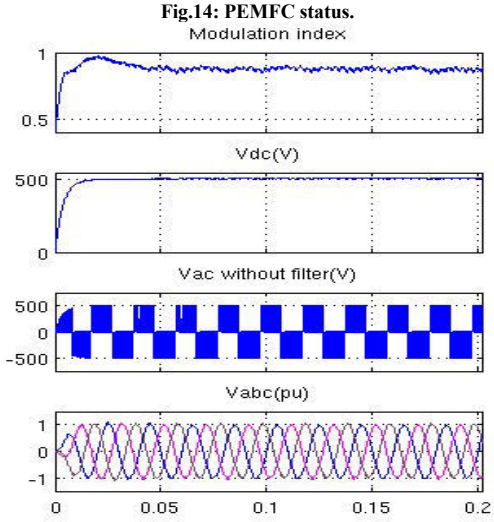

Fig.15:Inverter input V_{dc},Output V_{ac} and load voltage.

VI. CONCLUSION

The modeling and control fraimework of the PVBFC system is developed and simulated in MATLAB/ SIMULINK using SPS library. The simulation results give encouraging output on the performance of PVBFC integrated system and thus validate the effectiveness of the system. . The battery and the fuel cell power system have a great potential for being co-ordinated with the PV generator to smooth out the photovoltaic power's fluctuations. The battery and fuel cell back-up generators for PV power are able to ensure a continuous 24-hour power supply. From the research study, the DGS concept is identified as a potential field of research that determines the future electrical generation and distribution network. For future work, it can be expanded to include other energy storage system, micro turbine system, wind power system etc. as the DERs running in different operational conditions which could be in island or grid-connected operation. This can also be expanded to integrated PV generator with Fuel cell to work in parallel and battery system could handle all the intermittent conditions.

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INCREASING THE SPEED OF (8-16BITS) TWO'S COMPLEMENT MULTIPLIERS

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Abstract— Two's complement multipliers are important for a wide range of applications. In this paper, we present a technique to reduce by one row the maximum height of the partial product array generated by a radix-4 Modified Booth Encoded multiplier, without any increase in the delay of the partial product generation stage. This reduction may allow for a faster compression of the partial product array and regular layouts. This technique is of particular interest in all multiplier designs, but especially in short bit-width two's complement multipliers for high-performance embedded cores. The proposed method is general and can be extended to higher radix encodings, as well as to any size square and m_ n rectangular multipliers. We evaluated the proposed approach by comparison with some other possible solutions; the results based on a rough theoretical analysis and on logic synthesis showed its efficiency in terms of both area and delay.

Keywords- Terms—Multiplication, Modified Booth Encoding, partial product array.

I. INTRODUCTION

In multimedia, 3D graphics and signal processing applications, performance, in most cases, strongly depends on the effectiveness of the hardware used for computing multiplications, since multiplication is, besides addition, massively used in these environments. The high interest in this application field is witnessed by the large amount of algorithms and implementations of the multiplication operation, which have been proposed in the literature (for a representative set of references, see). More specifically, short bit-width (8-16 bits) two's complement multipliers with single-cycle throughput and latency have emerged and become very important building blocks for high-performance embedded processors and DSP execution cores. In this case, the multiplier must be highly optimized to fit within the required cycle time and power budgets. Another relevant application for short bit-width multipliers is the design of SIMD units supporting different data formats. In this case, short bit-width multipliers often play the role of basic building blocks. Two's complement multipliers of moderate bit-width (less than 32 bits) are also being used.
Massively in FPGAs. All of the above translates into a high interest and motivation on the part of the industry, for the design of high-performance short or moderate bit-width two's complement multipliers FPGAs. All of the above translates into a high interest and motivation on the part of the industry, for the design of high-performance short or moderate bit-width two's complement multipliers. The basic algorithm for multiplication is based on the well-known paper and pencil approach and passes through three main phases: 1) partial product (PP) generation, 2) PP reduction, and 3) final (carry-propagated) addition. During PP generation, a set of rows is generated where each one is the result of the product of one bit of the multiplier by the multiplicand. For example, if we consider the multiplication X.Y with both X and Y on n bits and of the form xn_1 . . . x0 and yn_1 . . . y0, then the ith row is, in general, a proper left shifting of yi . X, i.e., either a string of all zeros when yi = 0, or the multiplicand X itself when yi = 1. In this case, the number of PP rows generated during the first phase is clearly n.

Modified Booth Encoding (MBE) is a technique that has been introduced to reduce the number of PP rows, still keeping the generation process of each row both simple and fast enough. One of the most commonly used schemes is radix-4 MBE, for a number of reasons, the most important being that it allows for the reduction of the size of the partial product array by almost half, and it is very simple to generate the multiples of the multiplicand. More specifically, the classic two's complement n x n bit multiplier using the radix-4 MBE scheme, generates a PP array with a maximum height Of [n/2] +1 rows, each row before the last one being one of the following possible values: all zeros, +/-X;+/-2X. The last row, which is due to the negative encoding, can be kept very simple by using specific techniques integrating two's complement and sign extension prevention .

The PP reduction is the process of adding all PP rows by using a compression tree. Since the knowledge of intermediate addition values is not important, the outcome of this phase is a result represented in redundant carry save form, i.e., as two rows, which allows for much faster implementations. The final (carry-propagated) addition has the task of adding these two rows and of presenting the final result in a non redundant form, i.e., as a single

Presenting the final result in a non redundant form, i.e., as a single row.

In this work, we introduce an idea to overlap, to some extent, the PP generation and the PP reduction phases. Our aim is to produce a PP array with a maximum height of [n/2] rows that is then reduced by the compressor tree stage

As we will see for the common case of values n which are power of two, the above reduction can lead to an implementation where the delay of the compressor tree is reduced by one XOR2 gate keeping a regular layout. Since we are focusing on small values of n and fast single-cycle units, this reduction might be important in cases where, for example, a high computation performance through the assembly of a large number of small processing units with limited computation capabilities is required, such as X 8 or 16 X16 multipliers.

TABLE 1
Modified Booth Encoding (Radix-4)

y_{2i+1}	y_{2i}	y_{2i-1}	Generated partial products
0	0	0	$0 \times X$
0	0	1	$1 \times X$
0	1	0	$1 \times X$
0	1	1	$2 \times X$
1	0	0	$(-2) \times X$
1	0	1	$(-1) \times X$
1	1	0	$(-1) \times X$
1	1	1	$0 \times X$

A similar study aimed at the reduction of the maximum height to [n/2] but using a different approach has recently presented interesting results in .and previously, by the same authors. Thus, in the following, we will evaluate and compare the proposed approach with the technique in Additional details of our approach, besides the main results presented here.

The paper is organized as follows: the multiplication algorithm based on MBE is briefly reviewed and analyzed. we describe related works. we present our scheme to reduce the maximum height of the partial product array by one unit during the generation of the PP rows. Finally, we provide evaluations and comparisons.

II. MODIFIED BOOTH RECODED MULTIPLIERS

In general, a radix-B $=2^b$ MBE leads to a reduction of the number of rows to about [n/b] while, on the other hand, it introduces the need to generate all the multiples of the multiplicand X, at least from –B/2 x X to B/2 x X. As mentioned above, radix-4 MBE is particularly of interest since, for radix-4, it is easy to create the multiples of the multiplicand 0, +/-X, +/-2X. In particular, +/- 2X can be simply obtained by single left shifting of the corresponding +/- X. It is clear that the MBE can be extended to higher radices, but the advantage of getting a higher reduction in the number of rows is paid for by the need to generate more multiples of X. In this paper, we focus our attention on radix-4 MBE, although the proposed method can be easily extended to any radix-B MBE.

From an operational point of view, it is well known that the radix-4 MBE scheme consists of scanning the multiplier operand with a three-bit window and a stride of two bits (radix-4). For each group of three bits (y_{2i+1}, y_{2i}, y_{2i-1}), only one partial product row is generated according to the encoding in Table 1. A implementation of the radix-4 MBE and of the corresponding possible implementation of the radix-4 MBE and of the corresponding partial product generation is shown in Fig. 1, which comes from a small adaptation of [Fig. 12b]. For each partial product row, Fig. 1a produces the one, two, and neg signals. These signals are then exploited by the logic in Fig. 1b, along with the appropriate bits of the multiplicand, in order to generate the whole partial product array. Other alternatives for the implementation of the recoding and partial product genera-tion can be found in among others.

As introduced previously, the use of radix-4 MBE allows for the (theoretical) reduction of the PP rows to [n/2], with the possibility for each row to host a multiple of y_i x X, with y_i is belongs to {0, +/-1, +/-2}. While it is straightforward to generate the positive terms 0, X, and 2X at least through a left shift of X, some attention is required to generate the terms X and 2X which, as observed in Table 1, can arise from three configurations of the y_{2i+1}, y_{2i}, and y_{2i-1} bits. To avoid computing negative encodings, i.e., X and 2X, the two's complement of the multiplicand is generally used. From a mathematical point of view, the use of two's complement requires extension of the sign to the leftmost part of each partial product row, with the consequence of an extra area overhead. Thus, a number of strategies for preventing sign extension have been developed. The array resulting from the application of the sign extension prevention technique in to the partial product array of a 8 X 8 MBE multiplier is shown in Fig. 2.

The use of two's complement requires a neg signal (e.g., neg_0, neg_1, neg_2, and neg_3 in Fig. 2) to be added in the LSB position of each partial product row for generating the two's complemented as needed .thus, although for a nXn multiplier only [n/2] partial Of product [n/2] +1

When 4-to-2 compressors are used, which is a widely used option because of the high regularity of the resultant circuit layout for n power of two, the

reduction of the extra row may require an a
An additional delay of two XOR2 gates. By properly connecting partial product rows and using a Wallace reduction tree.

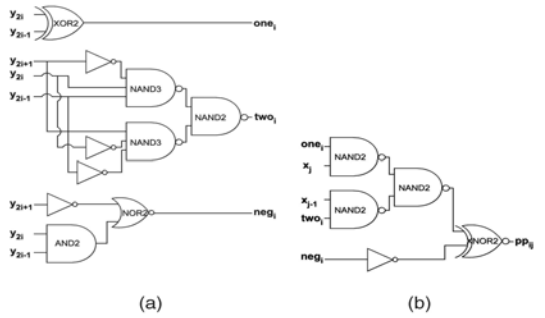

Fig. 1. Gate-level diagram for partial product generation using MBE (a) MBE signals generation. (b) Partial product generation.

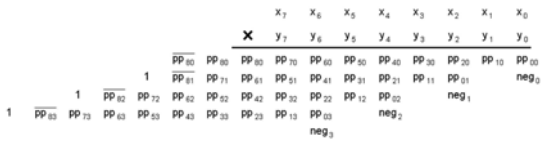

Fig. 2. Application of the sign extension prevention measure on the partial product array of a 8 X8 radix-4 MBE multiplier

the extra delay can be further reduced to one XOR2,. However, the reduction still requires additional hardware, roughly a row of n half adders. This issue is of special interest when n is a power of two, which is by far a very common case, and the multiplier's critical path has to fit within the clock period of a high performance processor. For instance, in the design presented in , for n = 16, the maximum column height of the partial product array is nine, with an equivalent delay for the reduction of six XOR2 gates . For a maximum height of the partial product array of 8, the delay of the reduction tree would be reduced by one XOR2 gate. Alternatively, with a maximum height of eight, it would be possible to use 4 to 2 adders, with a delay of the reduction tree of six XOR2 gates, but with a very regular layout. the reduction still requires additional hardware, so we use MBE in this it will reduce the area, time and increase the the power this paper satisfies the vlsi (very large scale integration) design.

III. RELATED WORKS

Some approaches have been proposed aiming to add the[n/2]+1 rows, possibly in the same time as the [n/2]rows. The solution presented is based on the use of different types of counters, that is, it operates at the level of the PP reduction phase. Kang and Gaudiot propose a different approach in that manages to achieve the goal of eliminating the extra row before the PP reduction phase. This approach is based on computing the two's complement of the last partial product, thus eliminating the need for the last neg signal, in a logarithmic time complexity. A special tree structure (basically an incrementer implemented as a prefix tree) is used in order to produce the two's complement (Fig. 3), by decoding the MBE signals through a 3-5 decoder (Fig. 4a). Finally, a row of 4-1 multiplexers with implicit zero output[1] is used (Fig. 4b) to produce the last partial product row directly in two's complement, without the need for the neg signal. The goal is to produce the two's complement in parallel with the computation of the partial products of the other rows with maximum overlap. In such a case, it is expected to have no or a small time penalization in the critical path. The architecture is a logarithmic version of the linear method presented and With respect to the approach in is more general, and shows better adaptability to any word size. An example of the partial product array produced using the above method is depicted in Fig. 5. In this work, we present a technique that also aims at producing only [n/2] rows, but by relying on a different approach

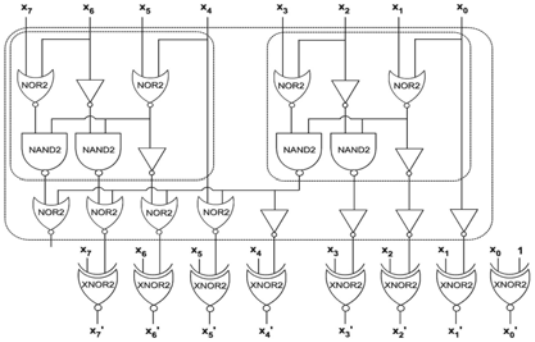

Fig. 3. Two's complement computation (n = 8)

IV. BASIC IDEA

The case of n x n square multipliers is quite common, as the case of n that is a power of two. Thus, we start by focusing our attention on square multipliers, and then present the extension to the general case of m n rectangular multipliers.

1.1 Square Multipliers

The proposed approach is general and, for the sake of clarity, will be explained through the practical case of 8 x 8 multiplications (as in the previous figures). As briefly outlined in the previous sections, the main goal of our approach is to produce a partial product array with a maximum height of [n/2] rows, without introducing any additional delay

Let us consider, as the starting point, the form of the simplified array as reported in Fig. 2, for all the partial product rows except the first one. As depicted in Fig. 6a, the first row is temporarily considered as being split into two sub rows, the first

one containing the partial product bits (from right to left) from pp_{00} to $pp_{80(bar)}$ and the second one with two bits set at "one" in positions 9 and 8. Then, the bit neg_3 related to the fourth partial product row, is moved to become a part of the second sub row. The key point of this "graphical" transformation is that the second sub row containing also the bit neg_3, can now be easily added to the first sub row, with a constant short carry propagation of three positions (further denoted as "3-bits addition"), a value which is easily shown to be general, i.e., independent of the length of the operands, for square multipliers. In fact, with reference to the notation of Fig. 6, we have that $qq_{90(bar)}$ qq_{90} qq_{80} qq_{70} qq_{60} =0 0 pp_{80} (bar) pp_{70} pp_{60} + 0 1 1 0 neg3 . As introduced above, due to the particular value of the second operand, i.e., 0 1 1 0 neg_3, in , we have observed that it requires a carry propagation only across the least-significant three positions, a fact that can also be seen by the implementation shown in Fig. 7.

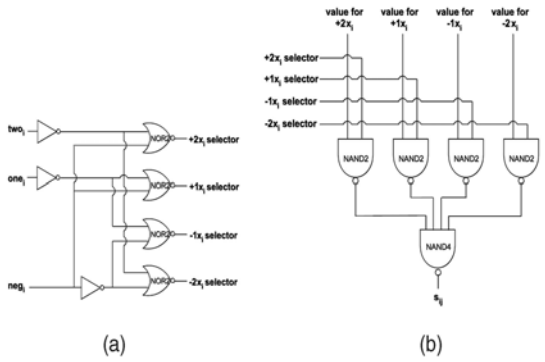

Fig. 4. Gate-level diagram for the generation of two's complement partial product rows. (a) 3-5 decoder. (b) 4-1 multiplexer.

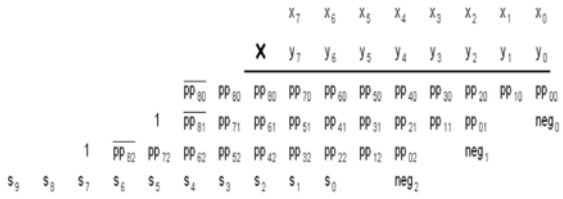

Fig. 5. Partial product array by applying the two's complement computation method in to the last row.

It is worth observing that, in order not to have delay penalizations, it is necessary that the generation of the other rows is done in parallel with the generation of the first row cascaded by the computation of the bits qq90(bar) qq90 qq80 qq70 qq60 in Fig. 6b. In order to achieve this, we must simplify and differentiate the generation of the first row with respect to the other rows. We observe that the Booth recoding for the first row is computed more easily than for the other rows, because the y_{-1} bit used by the MBE is always equal to zero. In order to have a preliminary

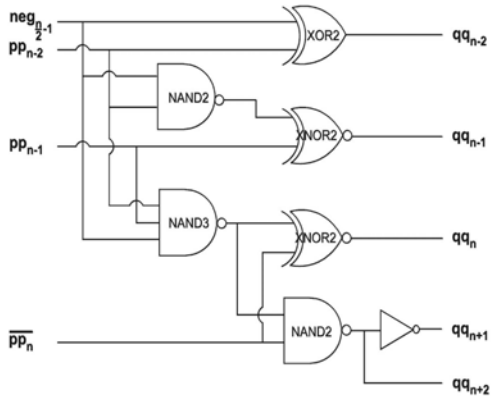

Fig. 6. Partial product array after adding the last neg bit to the first row.
(a) Basic idea. (b) Resulting array.

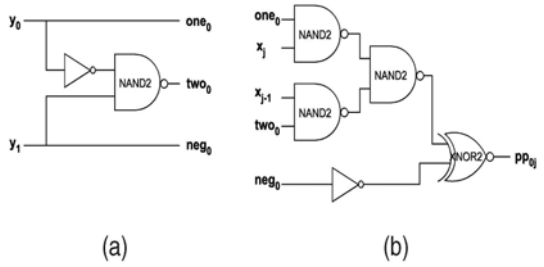

Fig. 7. Gate-level diagram of the proposed method for adding the last neg bit in the first row.

Analysis which is possibly independent of technological details, we refer to the circuits in the following figures:

. Fig. 1, slightly adapted from , for the partial product generation using MBE;

. Fig. 7, obtained through manual synthesis (aimed at modularity and area reduction without compromising the delay), for the addition of the last neg bit to the three most significant bits of the first row;

. Fig. 8, obtained by simplifying Fig. 1 (since, in the first row, it is $y_{2i-1} = 0$), for the partial product generation of the first row only using MBE; and
Fig. 9, obtained through manual synthesis of a combination of the two parts of Fig. 8 and aimed at decreasing the delay of Fig. 8 with no or very small area increase, for the partial product genera-tion of the first row only using MBE.

In particular, we observe that, by direct comparison of Figs. 1 and 8, the generation of the MBE signals for the first row is simpler, and theoretically allows for the saving of the delay of one NAND3 gate. In addition, the implementation in Fig. 9 has a delay that is smaller than the two parts of Fig. 8, although it could require a small amount of additional area. As we see in the following, this issue hardly has any significant impact on the overall design, since this extra hardware is used only for the three most significant bits of the first row, and not for all the other bits of the array.

The high-level description of our idea is as follows:

1. Generation of the three most significant bit weights of the first row, plus addition of the last neg bit:
Possible implementations can use a replication of three times the circuit of Fig. 9 (each for the three most significant bits of the first row), cascaded by the circuit of Fig. 7 to add the neg signal;

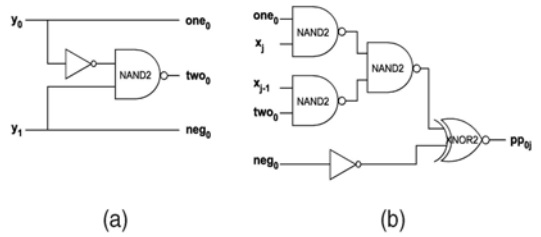

Fig. 8. Gate-level diagram for first row partial product generation.
(a) MBE signals generation. (b) Partial product generation.

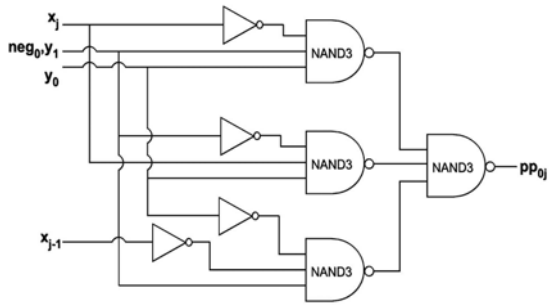

Fig. 9. Combined MBE signals and partial product generation for the first row (improved for speed).

2. Parallel generation of the other bits of the first row: possible implementations can use instances of the circuitry depicted in Fig. 8, for each bit of the first row, except for the three most significant;
3. Parallel generation of the bits of the other rows: possible in implementations can use the circuitry of Fig. 1, replicated for each bit of the other rows.

All items 1 to 3 are independent, and therefore can be executed in parallel. Clearly if, as assumed and expected, item 1 is not the bottleneck (i.e., the critical path), then the implementation of the proposed idea has reached the goal of not introducing time penalties.

1.2 Extension to Rectangular Multipliers

A number of potential extensions to the proposed method exist, including rectangular multipliers, higher radix MBE, and multipliers with fused accumulation. Here, we quickly focus on a m X n rectangular multipliers. With no loss of generality, we assume m >= n, i.e. m =n+m' with m'>=0, since it leads to a smaller number of rows; for simplicity, and also with no loss of generality, in the following, we assume that both m and n are even. Now, we have seen in Fig. 6a, that for m'= 0 then the last neg bit, i.e., $neg_{n/2-1}$ belongs to the same column as the first row partial product $pp_{n-2;0}$. We observe that the first partial product row has bits up to $pp_{m;0(bar)}$; therefore, in order to also include in the first row the contribution of negn/2-1, due to the particular nature of operands it is necessary to perform a(m'+3)-bit addition in the sum qqm+10(bar)qqm+10qqm,0 . . . qqn-2,0 =00ppm,0(bar) . . ppn-2,0 +0 1 1. . . 0 negn/2-1. Thus, for rectangular multipliers, the proposed approach can be applied with the cost of a(m'+3)-bit addition The complete or even partial execution overlap of the first row with other rows generation clearly depends on a number of factors, including the value of m' and the way that the (m'+3)-bit addition is implemented, but still the proposed approach offers an interesting alternative that can possibly be explored for designing and implementing rectangular multipliers

V. ACKNOWLEDGMENTS

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CONCLUSIONS

Two's complement n x n multipliers using radix-4 Modified Booth Encoding produce [n/2] partial products but due to the sign handling, the partial product array has maximum height of [n/2]+ 1.We presented a scheme that produces a partial product array with a maximum height of [n/2], without introducing any extra delay in the partial product generation stage. With the extra hardware of a (short) 3-bit addition, and the simpler generation of the first

partial product row, we have been able to achieve a delay for the proposed scheme within the bound of the delay of a standard partial product row generation. The outcome of the above is that the reduction of the maximum height of the partial product array by one unit may simplify the partial product reduction tree, both in terms of delay and regularity of the layout. This is of special interest for all multipliers, and especially for single-cycle short bit-width multipliers for high performance embedded cores, where short bit-width multiplications are common operations.

We have also compared our approach with a recent proposal with the same aim, considering results using a widely used industrial synthesis tool and a modern industrial technology library, and concluded that our approach may improve both the performance and area requirements of square multiplier designs. The proposed approach also applies with minor modifications to rectangular and to general radix-B Modified Booth Encoding multipliers.

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DENSITY FUNCTIONAL THEORY STUDIES OF ELECTRONIC AND THERMAL PROPERTIES OF ZNSIP SEMICONDUCTOR

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Abstract— First principles calculation within density functional theory (DFT) has been used to calculate the electronic, optical and thermal properties of $ZnSiP_2$ chalcopyrite semiconductor. The result of band structure, total density of state (DOS) and partial density of state (PDOS) have been discussed. The dielectric constant, refractive index, reflectivity, absorption coefficients, extinction coefficient and loss function have been presented in energy range of 0-25 eV. The values of melting point, Debye temperature, heat of formation and bulk modulus have been calculated. The calculated values of these parameters are in good agreement with the experimental values and the value reported by previous researchers.

Keywords- DFT; Electronic structure; Optical properties; Thermal properties

I. INTRODUCTION

During last few decades considerable amount of experimental and theoretical work has been done to understand the various electronic and thermal properties of I-III-VI_2 and II-IV-V_2 groups of chalcopyrite semiconductors because of their wide applications in the fields of linear and nonlinear optical devices [1]. Several workers have used different techniques such as density functional theory (DFT) [2-7], full potential linear augmented plane wave plus local orbit method (FP-LAPW+lo) [8-9] and X-ray diffraction [10] to investigate the electronic, optical and thermal properties of these chalcopyrites. Kumar et al. [11-13] have explained these properties using plasma oscillation theory of solids. Among these large families of chalcopyrites, $ZnSiP_2$ is a promising material for high power optical frequency conversion in the near and mid-infrared regions. In this paper, we have studied the properties of $ZnSiP_2$ semiconductor using first-principles calculations within density functional theory (DFT) and calculated the band gap (E_g), dielectric constant, refractive index, absorption coefficients, bulk modulus (B), melting temperature (T_m), Debye temperature (θ_D), plasmon energy $(\hbar\omega_p)$, heat of formation $(-\Delta H_f)$. Our calculated values of these parameters are in fair agreement with the available experimental values and the values reported by different workers.

II. COMPUTATIONAL DETAILS

Using Cambridge Sequential Total Energy Package (CASTEP) simulation software, we have calculated various parameters of $ZnSiP_2$ material. The calculations are based on the local density approximation (LDA) with exchange-correlation Ceperley-Alders potential parameterized by Perdew-Zunger scheme, with Norm-conserving Pseduo-potentials using plane wave basis set cut-off at 400 eV. Optimized structure has been obtained by applying Broyden, Fletcher, Goldfarb and Shannnon (BFGS) schemes. For this method, crystal reciprocal-lattice and integration over the Brillouin zone have been performed using 5 x 5 x 2 Monkhorst-pack. During the geometry optimization, the total energy difference of $5x10^{-7}$ eV/atom, Hellmann-Feynman ionic force within 0.01 eV/A°, maximum stress within $0.02\ GPa$ and maximum displacement within $5x10^{-4}\ A^\circ$ have been taken.

III. RESULT AND DISCUSSION

a. The electronic and band structure of $ZnSiP_2$

The tetrahedrally coordinated $ZnSiP_2$ semiconductor belongs to the space group $I\bar{4}2d$ (No. 122) with body-centered tetragonal structure having four formula units in each unit cell [1]. This chalcopyrite is analogous to III-V compounds and is a super-lattice of zincblende structure. The atomic positions of $ZnSiP_2$ crystal are Zn (0, 0, 0), Si (0, 0, 0 .5) and P (u, 0.25, 0.125), where u is the lattice constant. We have performed band structure calculation using local density approximation (LDA) method. The band structure of $ZnSiP_2$ is shown in Fig. 1, which shows that the calculated value of energy gap 0f $ZnSiP_2$ is 1.383 eV. This value of energy gap is obtained using LDA scheme, which is slightly less than the experimental value of 2.07 eV [5]. The calculated, experimental and reported values of energy gaps are listed in Table 1**.** Further, it is well known that the LDA method underestimates the value of energy gap [3]. To overcome this problem, a well known technique, called the scissor correction, is used [14] which makes the calculated value equals to experimental value. Our calculated value of E_g is scissor corrected by 0.687 eV for LDA scheme.

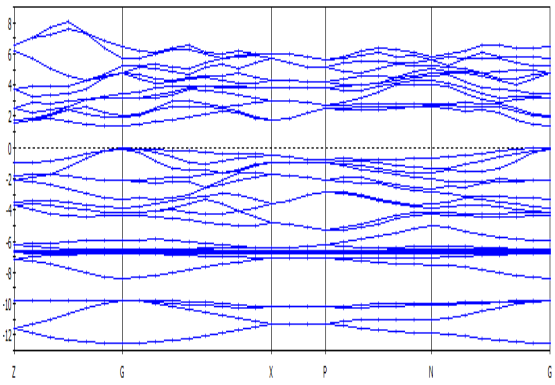

Fig. 1. Band structure of $ZnSiP_2$.

Fig. 2 shows the total density of state (TDOS) and partial densities of state (PDOS) for Zn-s/d, Si-s/p and P-s/p of $ZnSiP_2$ semiconductor. The PDOS signifies the angular momentum character, the orbital character and the states of hybridization of the semiconductor. The valence band maximum (VBM) is due to the presence of P-s/p, Zn-d, and Si-s/p, while conduction band minimum (CBM) is dominated by P-p and Si-p states, and little contribution of Si-s and P-s states. Further, the PDOS can be formally divided into three parts. The first part is from -12.8 eV to -9 eV which depends upon P-s and Si-s/p states, the second part is from -8.3 eV to Fermi energy (E_F), which are mainly due to the Si-p, Zn-d and P-p states, and finally the last part which comes under conduction band essentially dominated by P-p and Si-p states with minor presence of Si-s. From the Fig. 2, we can conclude that their exist a strong interaction between P-p and Si-p at around -3 eV.

The numerical value of plasmon energy $(\hbar\omega_p)$ of $ZnSiP_2$ semiconductor has been calculated from the loss function vs energy graph (see section III (B)), which comes out to be 15.95 eV against the reported value of

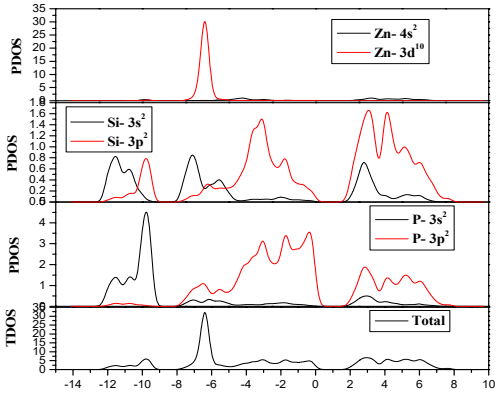

Fig.2. Total density of states (TDOS) and partial density of states (PDOS) of $ZnSiP_2$.

17.02 eV [12]. Using this value of plasmon energy (15.95 eV), we have further calculated the values of various parameters such as bulk modulus (B), melting point (T_m), Debye temperature (θ_D) and heat of formation $(-\Delta H_f)$ of $ZnSiP_2$ from the relations between $\hbar\omega_p$ and these parameters proposed by the author in their earlier publications [11,12,13]. The calculated values of these parameter are listed in Table 1 along with the experimental values and the values reported of different researchers. A fairly good agreement has been obtained between them.

Table 1: The energy gap (E_g), bulk modulus (B), melting temperature (T_m), Debye temperature (θ_D), plasmon energy $(\hbar\omega_p)$, heat of formation $-(\Delta H_f)$ of $ZnSiP_2$ semiconductor.

* This work, [a]Ref 5, [b]Ref 13, [c]Ref 15, [d]Ref 16, [e]Ref 12, [f]Ref 17, [g]Ref 8.

Compd.	**E_g (eV)**	**B (GPa)**	**T_m (K)**	**(θ_D) (K)**	**$(\hbar\omega_p)$ (eV)**	**$-(\Delta H_f)$**	**$\varepsilon_1(0)$**	**n(0)**
$ZnSiP_2$	1.325* 2.07[a]	80.98* 79.00[c] 93.13[b] 88.00[d]	1250.8* 1572.6[e]	354.58* 444.79[e]	16.03* 17.02[b]	287.1* 307.8[f]	11.87* 11.24[g]	3.4* 3.4[d]

b. Optical properties

The optical properties such as refractive index $n(\omega)$, reflectivity $R(\omega)$, extinction coefficient $k(\omega)$, absorption coefficient $I(\omega)$, and energy loss function $L(\omega)$ of $ZnSiP_2$ material can be measured from complex dielectric function $\varepsilon(\omega)$. In the presence of electric field $\vec{E}$ the frequency dependent dielectric function $\varepsilon(\omega)$ is divided into two bands: the interband and the intraband transitions. The information related to the intraband transition is useful for the metals and the interband transition is useful for the semiconductors. The interband transition is further divided into two bands: the direct band and the indirect band transitions. With the help of momentum matrix elements between occupied and unoccupied wave functions, it is possible to calculate the direct interband contribution to the imaginary part of dielectric function $\varepsilon_2(\omega)$. The real part of dielectric function $\varepsilon_1(\omega)$ can be calculated using the following Kramer-Kroning relations:

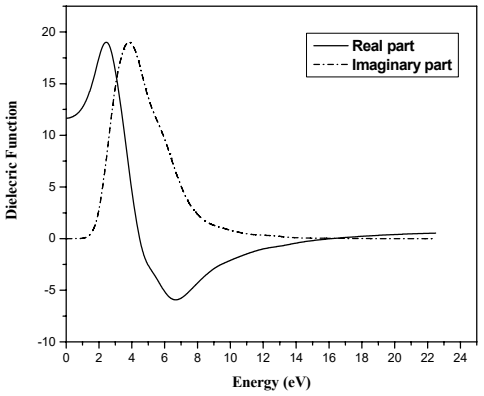

Fig. 4. Imaginary part $\varepsilon_2(\omega)$ (dash line) and real part $\varepsilon_1(\omega)$ (solid line) of the dielectric function of $ZnSiP_2$.

$$\varepsilon_1(\omega) = 1 + \frac{2}{\pi}\int_0^{\infty} \frac{\varepsilon_2(\omega)\omega' d\omega'}{\omega'^2 - \omega^2} \qquad (6)$$

$$\varepsilon_2(\omega) = \frac{Ve^2}{2\pi m^2 \omega^2}\int d^3k \sum_{nn'} \left|\langle kn|p|kn'\rangle\right| f(kn) \times [1 - f(kn')]\delta(E_{kn} - E_{kn'} - \hbar\omega) \qquad (7)$$

Figure 4 shows that the real and imaginary parts of dielectric constant, the real part $\varepsilon_1(0)$ = 11.87 for $ZnSiP_2$ against the reported value of 11.24 [8]. The calculated value of $\varepsilon_1(0)$ is found to be slightly higher in comparison to the theoretical value listed in Table 1. It is well known that experimental dielectric constant is absolute sum of electronic dielectric constant and lattice dielectric constant, and the lattice term cannot be neglected due to the ionic character present in $ZnSiP_2$. Also according to the Penn model, the static dielectric constant, $\varepsilon_1(0) = 1 + (\hbar\omega_p / E_g)^2$. This shows that the real part of dielectric function strongly depends on the energy gap of the semiconductor. The calculated energy gap is smaller than the experimental value due to the well known behavior of LDA method. Therefore, it is obvious that the calculated dielectric constant is slightly higher than the theoretical value. From the dielectric function, all other optical properties $n(\omega)$, $R(\omega)$, $k(\omega)$, $I(\omega)$, and $L(\omega)$ are expressed by previous researchers [4]. The calculated result of refractive index is shown in Fig. 5. The theoretical and experimental refractive indices of crystals are also listed in Table 1. The calculated values are in good agreement with experimental results.

For the calculation of absorption spectrum, reflectivity, extinction coefficient and energy-loss spectrum curves are plotted in Fig. 6 (a)-(d)**.** In these calculations we have considered the case of the absorption spectrum shown in Fig. 6(a), the incident radiation with the linear polarization along the [10 0] direction with smearing 0.5eV. Absorption spectrum shown in Fig. 6(a) explains the decay of light intensity in unit distance. The absorption edge is located at 4.2eV and rapidly decreases in the lower nergy band, which is well known behavior of semiconductors and insulators. The energy-loss function tells about the energy-loss of a fast electron traversing in the semiconductor. The point at which highest loss-function occur, i.e. 16.03 eV which corresponds to plasmon energy as shown in Fig. 6(d) and listed in Table 1**.**

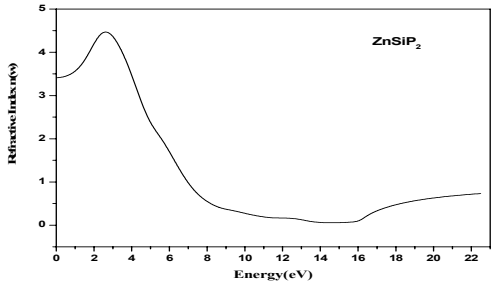

Fig. 5. Refractive index of $ZnSiP_2$.

At this point real and imaginary part of dielectric function is almost zero and corresponds to the trailing edge of Reflectivity spectra $R(\omega)$.

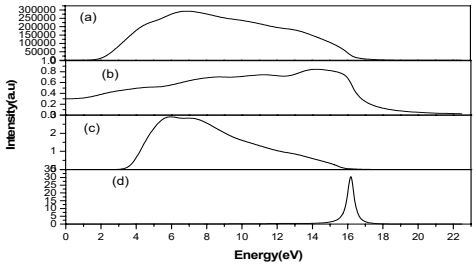

Fig.6. Optical constants of ZnSiP2: (a) absorption spectrum, (b) reflectivity, (c) extinction coefficient and (d) energy-loss spectrum.

CONCLUSION

The structural, electronic and optical properties of $ZnSiP_2$ compound have been calculated using CASTEP simulation software. We have performed first-principle calculation which is proven to be most accurate method for the computation of electronic structure of solids. The values of band gap, bulk modulus, heat of formation, Debye temperature, dielectric constant, refractive index and energy-loss spectra are in good overall agreement with the experimental values and the values reported by earlier researchers. So, the proposed theoretical calculations give a better agreement with the experimental values than the values proposed by earlier workers, which shows the soundness of the present simulation.

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SYNTHESIS OF LINEAR ANTENNA ARRAY FOR MINIMUM SIDE LOBE LEVEL USING SWARM INTELLIGENCE ALGORITHM

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Abstract: The synthesis of an antenna array uses the evolutionary algorithms like Genetic Algorithms and Particle Swarm Optimization techniques. Here in this paper Particle Swarm Optimization Technique is used to reduce the side lobe level. The PSO technique gives the best results in the reduction of side lobe level compared to that of the GA and Dolph Tschebyscheff's methods . The results of all the methods compared and it was found that PSO will yield the side lobe level up to less than -50dB which is much superior than that of the side lobe level obtained by using G.A. and Dolph Tschebyscheff's methods .

Keywords - GA - Gentic Algorithm. PSO- Particle Swarm Optimization.

I. INTRODUCTION

Antennas arrays synthesis is widely used in different communication systems phased array radar applications, satellite communications, sonar and wireless communication applications in which high power gain is required in the given direction. Considerable number of studies have been made on the antenna arrays where the array pattern of an antenna array should have high power gain in the given direction. The expected array pattern can be realized by choosing the physical placement of the antennas elements and their amplitude and phase of excitations. There are several mathematical techniques are adapted in the design of array to have the required side lobe level , phase and power of an antenna. But the mathematical techniques usually converge to local values rather than global optimum values. Hence there is need of stochastic techniques that are applied to the phased array antenna synthesis to minimize the side lobe level of an antenna array and these techniques produces best results than differential techniques. The problem of reducing the SLL of the given radiation pattern of an antenna array is the primary concern. The main advantage of the array antenna synthesis is to control the side lobe level to a possible minimum value. The synthesis of linear array antenna is difficult by using non-linear optimization methods. There are different classical methods to solve the problem of reducing the side lobe level but all these methods are using mathematical models[1] which are limited in nature. Instead of using the direct method of finding the parameters of our interest which are limited in choice, the random or stochastic search methods i.e. PSO,GA are used. In our application PSO, GA[2] and Dolph Tschebyscheff's methods has been applied and results are compared. It was found that PSO algorithm produces SLL up to -50.7dB which is shown at the end.

II. ALGORITHM

Particle swarm optimization is the collective motion of flock of particles. Each member of the particle swarm is moved through a problem space by two elastic forces. The velocity and position which are updated at each time until the swarm as a whole is converges. The update rule in PSO contains two parameters. 1. The relative importance of the influences on a particle of the particle best and the swarm best solutions. 2. The number of particles is to be used as neighbor.

The PSO algorithm makes use of two independent random sequences, $r_1 \sim U(0,1)$ and $r_2 \sim U(0,1)$ these are used to effect the random nature of the algorithm given by the equ () . The values r_1 and r_2 are scaled by the constants $0 < c1,c2 \leq 2$. These constants are called the acceleration coefficients, and they influence the maximum size of the step that a particle can take in single iteration. The velocity update step is specified separately for dimension j $j \in 1...n$ so that v_{ij} denotes the j^{th} dimension of the velocity vector associated with the i^{th} particle.

$$y_i(t+1) = \begin{cases} y_i(t) & if \ \ f(x_i(t+1)) \geq f(y_i(t)) \\ x_i(t+1) & if \ \ f(x_i(t+1)) \leq f(y_i(t)) \end{cases} \quad (1)$$

x_i *is* the current position of the particle, v_i is the current velocity of the particle, y_i is the personal best position of the particle.

$$v_{ij}(t+1) = v_{ij}(t) + c_{1j}(t)[y_{ij}(t) - x_{ij}(t)] + c_2 r_{2j}(t)[y_j(t) - x_{ij}(t)] \quad (2)$$

The equation again simplified as

$$v_i(t) = wv_i(t-1) + c_1[P_i - x_i(t-1)] + c_2[P_g - x_i(t-1)] \quad (3)$$

Where P_i is the best position found by the particle i and P_g is the best position among all

particles. c_1 and c_2 are the variables representing the cognitive parameter and social parameter respectively. '*w*' is the inertia factor which improves the performance of the algorithm. The inertia factor decreases linearly with increase in the number of iterations. The position of the each particle is updated at every iteration by using the velocity vector by the equ.(4).

$$x_i(t)=x_i(t-1)+v_i(t) \quad (4)$$

For the i[th] particle the position is expressed as $X_i = (x_{i1}, x_{i2}, x_{i3}, x_{i4}, \dots\dots\dots\dots, x_{in})$ and the velocity is expressed as $V_i = (v_{i1}, v_{i2}, v_{i3}, v_{i4}, \dots\dots\dots\dots, v_{in})$.

PSO is a class of evolutionary algorithms based on random population. In the PSO algorithm each potential solution is associated with the random velocity in the initialization process; potential solutions are designated as particles.

III. PROBLEM FORMULATION

The array factor of any linear array having 'N' number of isotropic sources is given by the formula (4)

$AF(\theta) = \sum_{n=1}^{N} a_n e^{j\psi}$ here $\Psi = k\, d\, cos(\theta) + \beta$ (4)

k = wave number
N = number of elements.
a_n *= excitation coefficients.*
β *= Phase shift.*

The geometry of N number of isotropic sources located along the 'z' axis is shown in the fig. 1.

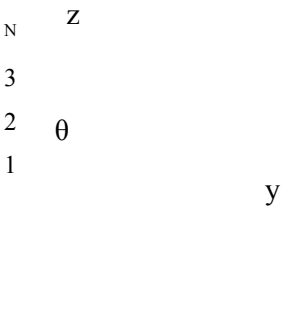

Fig.1 Linear phased array of 2N number of elements along the 'z' axis.

The array factor of the geometry given above is given by the formula (5)

$$AF(\theta) = 2\sum_{m=1}^{N} I_m \cos(kz_n \cos(\theta)) \quad (5)$$

The phased array antenna optimization is a complex problem as it consists of various parameters like side lobe level, polarization, impedance, beam width etc. In the present problem it is considered to optimize the excitation levels for minimum side lobe level of an array by keeping the remaining parameters constant. There are several classical approaches to minimize the side lobe level. Apart from these classical methods the new evolutionary techniques will also produces impressed results.

In the present problem we have considered 16 elements and the weights of these elements are selected randomly. The selected random weights are given as input to the fitness function so that the excitation levels converge to have a minimum side lobe level for a given antenna array. The fitness function i.e. SLL = [Main Lobe – First Side Lobe] in dB to calculate the depth of the side lobe level. After applying the optimization technique it converges to a minimum lobe level of -50.72dB by optimizing the excitation coefficients of an antenna array. The results are given at the end in the table 1.

The results of the optimization study was compared against Genetic algorithm optimization and Dolph Tschebyscheff's methods. T he excitation coefficients of the three cases are depicted in table 1. However after comparing all the three techniques PSO produces better results in reducing the side lobe level up to -50.72dB. The results of the three algorithms for radiation patterns and excitations are given at the end.

IV. CONCLUSIONS

This paper illustrates the simulation and desing of non uniform aray antenna for minimum side lobe level using Particle Swarm Optimization methods . There are several methods in the desing is propoased earlier among them Particle Swarm Optimiation algorithm is used to optimize the excitation coefficients of an antenna arrray effectively to generate the required radiation patttern. The simulation results are given in the table 1. for PSO,GA and Dolph Tschebyscheff methods. The main focus of the future work will be aimed at dealing with the other parameters and constraints.

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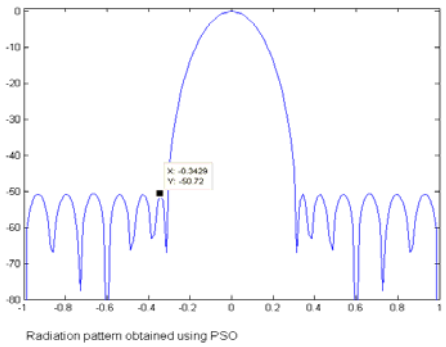
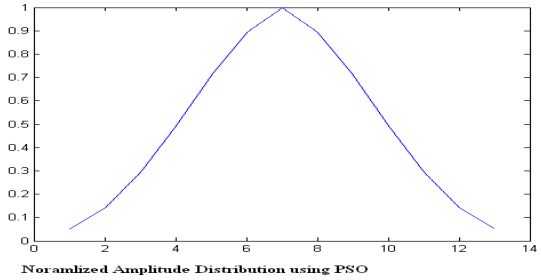
El. No.	PSO	GA	DCH
8,9	1.000	1.000	1.000
7,10	0.857	0.9286	0.935
6,11	0.647	0.797	0.816
5,12	0.445	0.649	0.661
4,13	0.280	0.434	0.492
3,14	0.148	0.327	0.332
2,15	0.055	0.171	0.196
1,16	0.000	0.0598	0.113
SLL	**50.72dB**	**- 37.58dB**	**-40dB**

Table 1 : Comparison of different algorithms for minimum side-lobe level and the excitation of current elements





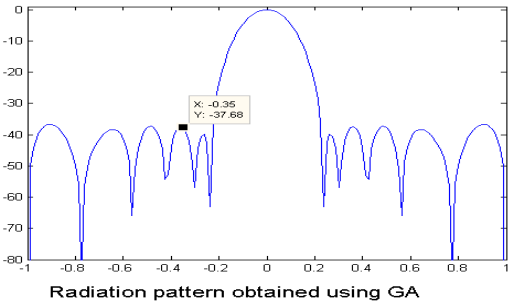


Fig 4 . Radiationpattern for 16 Elements using GA

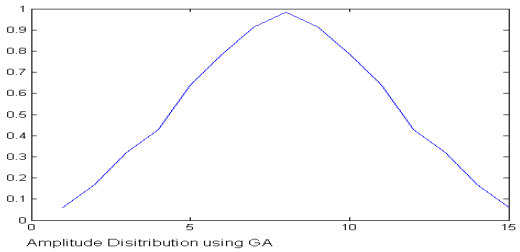


Fig 5. Excitation Coefficients of16 Elements using GA

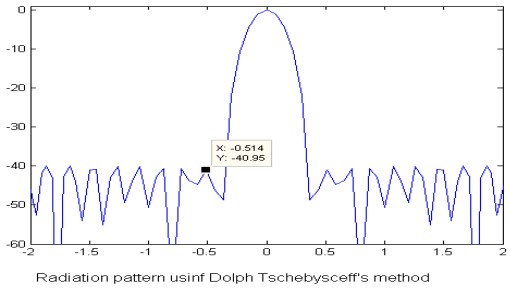


Fig 6 . Radiationpattern for 16 Elements using Dolph Tschebyscheff's method

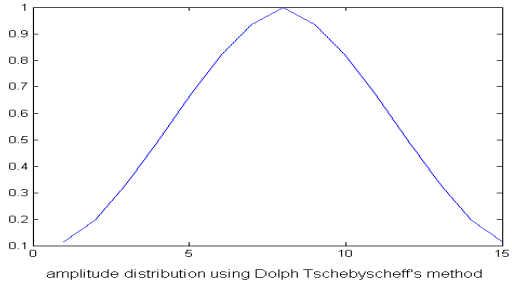


Fig 7. Excitation Coefficients of16 Elements using Dolph Tschebyscheff's method

AN EFFICIENT ANTI-COLLISION TECHNIQUE FOR RFID UHF TAG

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Abstract— This paper presents a proposed Reliable and Cost Effective Anti-collision technique (RCEAT) for Radio Frequency Identification (RFID) Class 0 UHF tag. The RCEAT architecture consists of two main subsystems; PreRCEAT and PostRCEAT. The PreRCEAT subsystem is to detect any error in the incoming messages. Then the identification bit (ID) of the no error packet will be fed to the next subsystem. The PostRCEAT subsystem is to identify the tag by using the proposed Fast-search Lookup Table. The proposed system is designed using Verilog HDL. The system is simulated using Modelsim and synthesized using Xilinix Synthesis Technology. The system has been successfully implemented in hardware using Field Programmable Grid Array (FPGA) Virtex II. The output waveforms from the FPGA have been tested on the Tektronix Logic Analyzer for real time verification. Finally the RCEAT architecture is resynthesized using Application Specific Integrated Circuit (ASIC) technology for on-chip implementation. This technology consists of 0.18 μm Library, Synopsys Compiler and tools. From the hardware verification results, it shows that the proposed RCEAT system enables to identify the tags without error at the maximum operating frequency of 180MHz. The system consumes 7.578 mW powers, occupies 6,041 gates and 0.0375 mm2 area with Data arrival time of 2.31 ns.

I. INTRODUCTION

In the data management system a significant role of the Data link layer is to convert the unreliable physical link between reader and tag into a reliable link. Therefore, the RFID system employs the *Cyclic Redundancy Check* (CRC) as an error detection scheme. The CRC calculation consists of an iterative process involving Exclusive-ORs and shift register which is executed much faster in hardware compare in software [9]. In addition for reader to communicate with the multiple tags, an anti-collision technique is required. The technique is to coordinate the communication between the reader and the tags. The common deterministic anti-collision techniques are based on the Tree algorithm such as the Binary Tree and the QueryTree algorithms [1]-[4]. However this technique has longer identification time which dependents on the number of existing tag and the identification bit (ID) length.

II. METHODOLOGY

In our proposed RCEAT the frame consists of slots and each slot (column) is divided into four minislots (rows). Therefore in each slot, four tags are allowed for contending the minislots. The RCEAT will identify these four tags using the proposed Lookup table. The uniqueness of this proposed technique is reducing the tag identification time in the Binary Tree. The existing tags are divided into four in each Read cycle to reduce the required iterations and thus faster the tag identification. This proposed technique does not require the tag to remember the instructions from the reader during the identification process. Thus the tag is treated as an address carrying device only and memory-less tag can be designed which requires very low power. The RCEAT identification methodology is shown in Fig. 1. In RCEAT, bidirectional communications are involved, from the reader to the tag (Downlink) and from the tag to the reader (Uplink). When the reader detects there are tags exist in its interrogation zone, it will power these tags. Then the reader sends the Select-group command based on the tag Prefix or Object Class (OC). The selected tags group will move to the Ready state. Next the Reader transmits Reset signals and its frame. After that the frame is transmitted back to the reader, column by column starting with the first column. This compensates the time required for transmitting the packet to the reader. Therefore for every Read cycle, there are always available packets at the reader waiting for identification. At the reader, the incoming packets for each link sequentially enter the RCEAT system. To avoid the four incoming packets from colliding with each other, these packets (IDs) are identified using the Binary Tree based technique with maximum four leaves. The reader selects these IDs using the proposed Fast-search Lookup table, and then the selected ID will be identified. Based on this proposed Lookup table, the four IDs will be identified rom the smallest value to the largest one in one Read cycle. Then the tag that has successfully identified will be acknowledged by sending the Kill-tag.

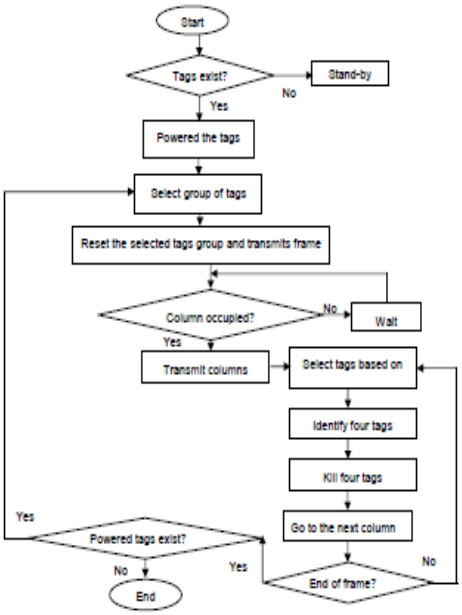


Fig. 1: RCEAT identification Methodology

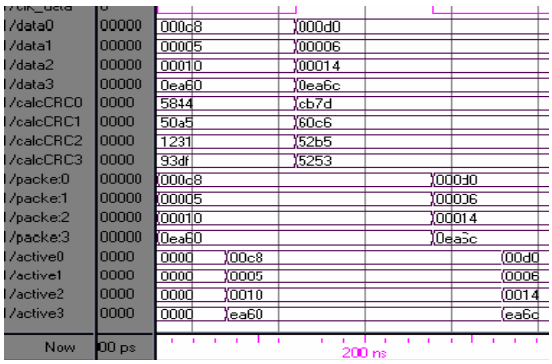
III. ARCHITECTURE

The RCEAT architecture consists of two subsystem; PreCLART and PostRCEAT (Fig. 4). In the PreRCEAT, the received messages are fed into the CRC-remover module. These received messages will be separated into two; the received packet and the received CRC. These packet and CRC are sent to the CRC checker module for verification process. The CRC checker module recalculated the CRC of the received packet. Then, this calculated CRC is compared with the received CRC. If the values are same, means no error, the status-bit is set to its original value i.e. zero. Otherwise or there are errors in the packet, the status-bit is set to two. After that, this updated status-bit is appended to its respective packet. Finally, the packet with the updated status-bit is fed to the Status-checker module. The Status-checker module will check any errors in the incoming packets. If there are errors, then reset the slot of the respective packet to zero value. Otherwise, fill the slot of the packet with its respective ID. The status-bit is removed from its packet and only the tag's ID will be output to the PostRCEAT [8]. In the PostRCEAT, the active tags are divided into a group of four for every Read cycle in order to reduce the number of iterations in the identification process.

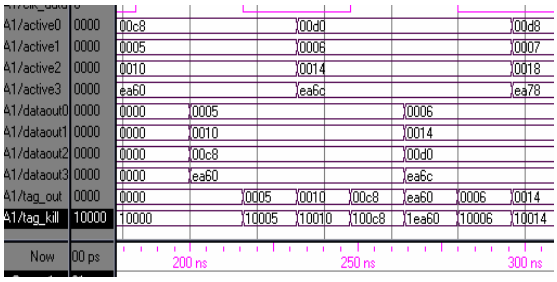
The PostRCEAT reads all the ID bits at once regardless of its length. This is performed by using the word-byword multiplexing. During the identification process, the Fast-search module identifies the four tag's IDs simultaneously in one Read cycle which equal to a Tag clock cycle. The module firstly identifies the smallest ID bits until the largest one follows the Binary Tree with a maximum number of four leaves.

IV. SIMULATION RESULTS

Verilog HDL codes for the RCEAT architecture have been successfully simulated and verified using the ModelSim XE II/Starter 5.7g tool. The following will discuss the Behavioral simulation waveforms for the selected ports in the RCEAT system as shown in Fig.2. At the first Read cycle, for the received messages of 000C8584416, 0000550A516, 00010123116, and 0EA6093DF16, the recalculated CRC of these messages are 584416, 50A516, 123116, and 93DF16 respectively. As a result, the calculated CRCs are equal to the received CRCs which are represented by the four bit of the least significant bit (LSB) of the messages. Since there are no errors in the received messages, the Status-bit of the packets are set to zero, which are represented by the MSB of the packets; 000C816, 0000516, 0001016 and 0EA6016 respectively. Finally, the ID of these packets will be fed simultaneously to the PostRCEAT subsystem. In the PostRCEAT subsystem, the Fast-search module will identify the four active tags simultaneously starting from the smallest value to the largest one. For examples, for the four input tag's ID of 00C816, 000516, 001016 and EA6016 will be identified as 000516, 001016, 00C816 and EA6016 respectively. Then these identified tags will be fed to the Read-killtag module simultaneously at the negative edge of the Tag clock. Finally, the Read-killtag Module will output the four identified tags serially, one tag at every cycle of the system clock starting from the smallest tag's ID to the largest one. Moreover, at the same clock cycle, the identified tag will be killed.



(a) PreRCEAT modules output

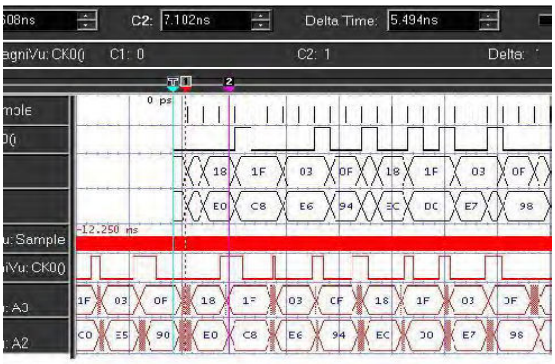


(b) PostRCEAT modules output

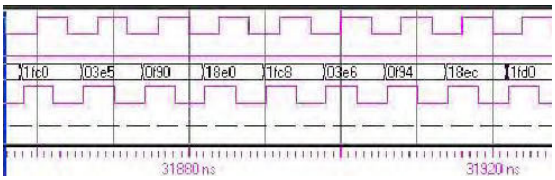
Fig. 2: The Behavioral simulation of RCEAT

V. IMPLEMENTATION AND VERIFICATION

The RCEAT architecture has been implemented in hardware using the Field Programmable Grid Array (FPGA) model Virtex II Xc2v250. The output waveforms from the FPGA have been displayed using the Tektronix Logic Analyzer model TLA 5201 for real time verification.



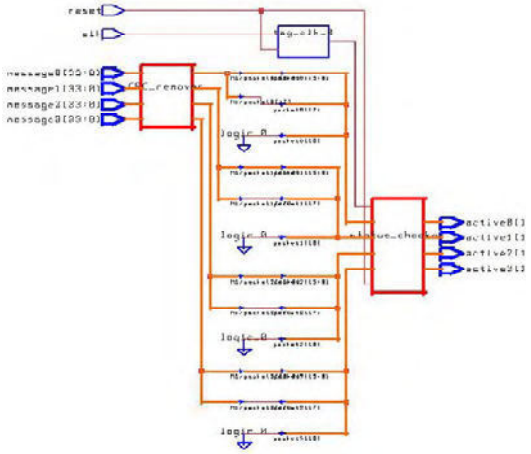
(a) PreRCEAT modules output



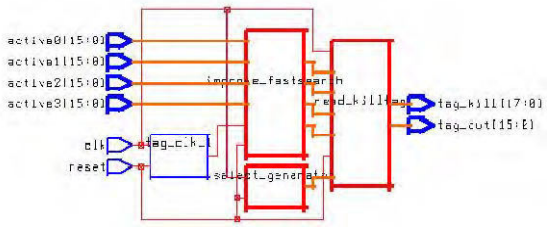
(b) RCEAT Place and Route simulation output

Fig. 3: RCEAT output at 180 MHz

From the result, it shows that the system still enables to identify the tags without errors at the operating frequency of 180 MHz. Fig. 3 shows the FPGA output and its equivalent place and route simulation result at this frequency. For examples for the first Read cycle the identified tags are 03E516, 0F9016, 18E016 and 1FC816 as marked by a circle.



(a) PreRCEAT block diagram



(b) PostRCEAT block diagram

Fig. 4: Synthesized block diagram of RCEAT

The RCEAT system has been successfully implemented in hardware using FPGA with desired performances. Then the system is implemented on chip using ASIC approach. In this approach the system is resynthesized using 0.18µm Library, Synopsys Compiler and tools. Table 1 shows the output parameters using two synthesis technology; Xilinix and ASIC. From the synthesis results, it shows the RCEAT architecture has the maximum operating frequency of 253 MHz and the total gates of 6,041. The average connection delay is 1.18 ns and the maximum pin delay is 5.35 ns. Moreover, the RCEAT occupies 0.03753 mm2 cell area and consumes 7.578 mW powers. The data required time and the data arrival time are 2.72 ns and 2.31ns respectively.

Table 1
Synthesis result parameters

Xilinix Parameters	ASIC Parameters
Max. Frequency=253MHz	Cell area= 0.03753 mm^2
Total gate count=6041	Power = 7.578 mW
Connection Delay=1.18ns	Arrival time=2.31ns
Max. pin Delay=5.35ns	Slack = 0.41 ns

CONCLUSIONS

A proposed Reliable and Cost Effective Anti-collision technique (RCEAT) is designed to achieve a reliable and cost effective identification technique of the tag. The RCEAT architecture consists of two main subsystems; PreRCEAT checks error in the incoming packets using the CRC scheme. PostRCEAT identifies the error free packets using Binary Tree based technique. The architecture has been synthesized using Xilinix Synthesis Technology (XST). The RCEAT architecture also has been successfully implemented in hardware using FPGA model Virtex II Xc2v250. The FPGA outputs have been verified in real time using Tektronix Logic Analyzer model TLA 520. Finally on chip verification has been done using 0.18 µm Silterra Library, Synopsys Compiler and tools. The result shows that the architecture has smaller cell area, power consumption and number of gates. Therefore minimize the implementation and operating costs.

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MODIFIED SVPWM FOR RENEWABLE ENERGY

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Abstract—The objective of the present work is to improve the output waveform of three level inverters used in in hybrid wind-solar energy system, where the switching frequency is very low. This is achieved by maintaining the synchronization, half-wave symmetry, quarter-wave symmetry, and three-phase symmetry in the pulse width modulation (PWM) waveforms. The principles of achieving synchronization and symmetries in terms of space vectors for three level inverters are presented. A novel synchronized space vector pulse width modulation (SVPWM) is showed by simulation results. The simulation waveforms of the inverter output voltage and no load current. The performance measure in terms of the weighted total harmonic distortion (THD) of the line voltage is computed for the linear modulation region.

Keywords—Harmonic distortion, induction motor drives, pulsewidth modulated inverters, pulsewidth modulation

I. INTRODUCTION

With increasing concern of global warming and the depletion of fossil fuel reserves, many are looking at sustainable energy solutions to preserve the earth for the future generations. Other than hydro power, wind and photovoltaic energy holds the most potential to meet our energy demands. Alone, wind energy is capable of supplying large amounts of power but its presence is highly unpredictable as it can be here one moment and gone in another. Similarly, solar energy is present throughout the day but the solar irradiation levels vary due to sun intensity and unpredictable shadows cast by clouds, birds, trees, etc. The common inherent drawback of wind and photovoltaic systems are their intermittent natures that make them unreliable

THREE level inverters have certain advantages over conventional two level inverters [1].

• Three level inverters can synthesize double the voltage levels using the devices of similar voltage rating. Hence, the power handling capacity can be doubled.

• For a given switching frequency, three level voltage canhave double the bandwidth.

• Three level inverters have improved total harmonic distortion (*THD*) compared to two level inverters.

Because of these features, three level inverters are finding application especially in medium voltage high-power drives.

In this conventional three level SVPWM scheme, *P*can take only 3,5,11,…values The major drawback of this scheme is that f_{sw}varies over a wide range with Fsin variable speed drives. In the case of conventional two level inverters, it is shown that the flexibility in selecting the space vectors results in design of SVPWM sequences which generate synchronized output waveforms with HWS, QWS, and TPS for any odd integer values of [6]. The objective of this paper is to exploit similar features of three level space vectors and design SVPWM sequences for three level inverter resulting in synchronized PWM outputs waveforms with HWS, QWS, and TPS. No such attempt is made in the literature in this direction and for the first time a novel synchronized three level SVPWM with waveform symmetries is proposed for low-switching frequency applications. Even though three level SVPWM is an active area of research, most of the work is focussed on specific issues related to conventional symmetrical SVPWM algorithm like simplifying the algorithm [7], implementation issues [8]–[11], reducing the switching losses [12], neutral point voltage balancing [13]–[18], or reducing common mode voltage [19].

The computational complexity of three level SVPWM can be reduced to that of two level SVPWM, as shown in [7] and is applied to conventional SVPWM algorithm. In the present work, the simplified method given in [7] is further modified so that computation of synchronized SVPWM sequences and implementation on digital controller using assembly program is simple and modular. In Section II, this modified simple approach to SVPWM is explained. The design of the three level SVPWM sequences require different approach compared to two level SVPWM techniques as there are additional redundancies in space vectors, zero vector is no longer the common vector for all the regions of space vector space and direct current (dc) bus balancing has to be maintained. The basic principle of the space vector approach to synchronization and symmetry and design of sequences is detailed in Section III. The present work shows that by proper design of SVPWM sequences it is possible to get synchronization and various waveform symmetries for any integervalues of *P*.the simulation results are shown in section IV which shows the three level output wave forms

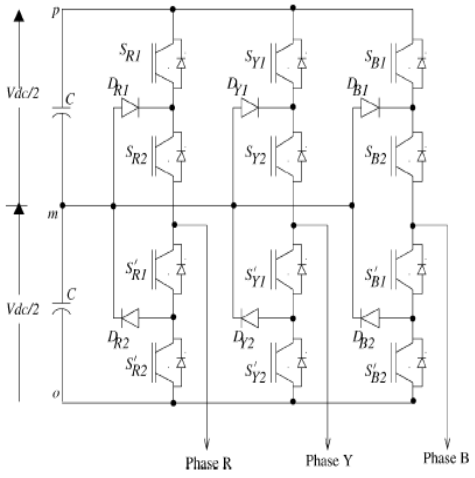


Fig. 1. Three level diode clamp inverter.

The performance of the proposed technique is studied overthe entire linear modulation region of the drive. A comparison in terms of the weighted *THD* of the output line voltage (V_{LWTHD})for the proposed synchronized SVPWM technique with waveform\ symmetries and conventional synchronized SVPWM technique shows that consideration of symmetry results in improved*THD*. Similarly, a comparison V_{LWTHD} of proposed synchronized SVPWM with waveform symmetries and synchronized SPWM technique with waveform symmetries proves the superiority of the present method over synchronized SPWM technique. Also the variation of V_{LWTHD} as a function of *P*is studied and this result can be used for the optimal design of PWM technique in order to achieve minimum *THD*. A major requirement of three level PWM sequences is that the dc bus capacitor voltages must be balanced. It is shown that the proposed technique ensures the dc link capacitor voltage balancing over (1/3)*rd*cycle of the fundamental. This is an important result because the proposed method is simple, do not require any additional computation or feed back signal comparedto other methods presented in the literature [13]–[18]. The proposedmethod also results in minimum common mode voltage. Compared to the other three level SVPWM algorithms, the present work has a unique feature that it addresses all the major issues related to the three level PWM techniques such as computational complexity, synchronization, *THD*, dc bus voltage balancing, and common mode voltage. Hence, the proposed SVPWM method will be suitable for high-power applications
as it eliminates sub-harmonics by maintaining synchronization,
improves*THD* through various waveform symmetries, results in balanced dc bus voltage, and low common mode voltage.

TABLE I
DIODE CLAMP INVERTER: SWITCH STATUS AND DEFINITION OF STATE FOR POLE R

Switch status	State	Pole voltage
$S_{R1}=ON, S_{R2}=ON,$ $S'_{R1}=OFF, S'_{R2}=OFF,$ $D_{R1}=OFF, D_{R2}=OFF$	+1	$V_{Rm}=\frac{V_{dc}}{2}$
$S_{R1}=OFF, S_{R2}=ON,$ $S'_{R1}=ON, S'_{R2}=OFF,$ D_{R1} or D_{R2} will conduct depending on the polarity of the load current	0	$V_{Rm}=0V$
$S_{R1}=OFF, S_{R2}=OFF,$ $S'_{R1}=ON, S'_{R2}=ON,$ $D_{R1}=OFF, D_{R2}=OFF$	−1	$V_{Rm}=-\frac{V_{dc}}{2}$

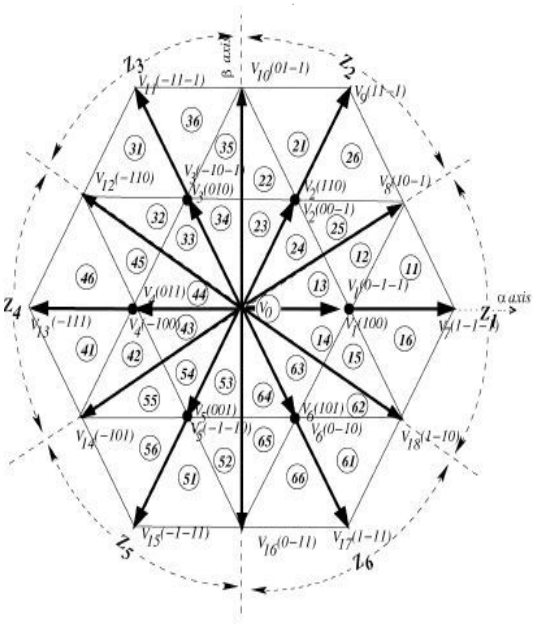


Fig. 2. Space vectors of three level inverter with sector and subsector definition.

II. SIMPLIFIED APPROACH TO SVPWM

Fig. 1 shows the circuit diagram of a three level diode clampinverter. The states are defined in Table I. The space vectorsassociated with the three level inverters on plane **α-β**are shown in Fig. 2. In the space vector approach to PWM, the reference vector is sampled at regular interval Ts. The sampled reference vector Vr is approximated by time averaging the nearest three vectorsVx,Vy ,andVz according to (1) and (2).

$$\overline{V}_r T_s = \overline{V}_x T_x + \overline{V}_y T_y + \overline{V}_z T_z \quad (1)$$

$$T_s = T_x + T_y + T_z \quad (2)$$

Where Tx ,Ty ,and Tzare the dwell times of Vx,Vy , and Vz,
respectively.Unlike two level inverters, the zero vector is no longercommon for all the regions. So solution to (1) and (2) involvessolving three simultaneous equations. In order to simplify

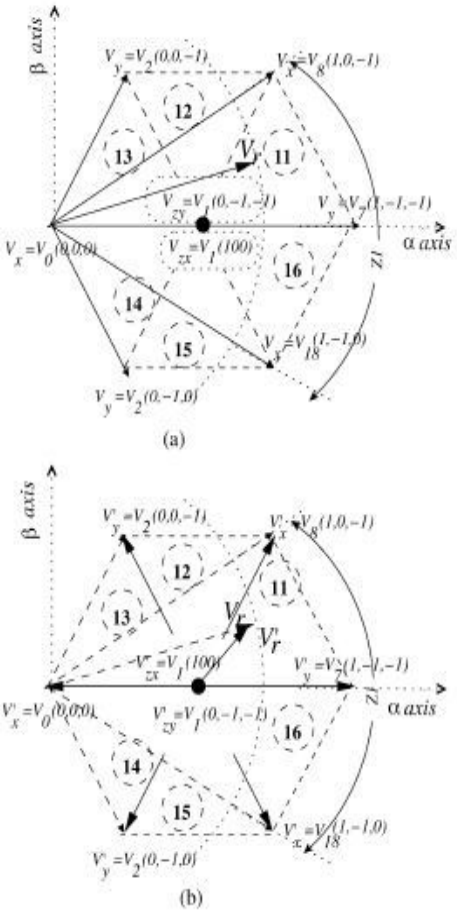


Fig. 3. (a) Vectors of sector 1. (b) Mapping of vectors of sector 1 to fictitious vectors.

the above equations, a simple approach based on the method given in [7] is adopted, in which the symmetry of the space vectors is exploited. The space vector plane is divided in to six
sectors, each of 60 , as shown in Fig. 2. Each sector , where Z=1,2,3,… is associated with one pivot vector $V_z$and six other vectors. The pivot vector $V_1$and other six vectors of sector 1 are redrawn in Fig. 3(a). The vectors of the other sectors are phase displaced by π/3 radians. All the six sectors exhibit symmetry. All the vectors associated with the given sector , can be mapped to a set of seven fictitious vectors with
V_1as the center as defined by (3). This is illustrated in Fig. 3(b)

$$\begin{aligned}\overline{V}'_r &= \overline{V}_r e^{j(Z-1)\pi/3} - \overline{V}_1\\ \overline{V}'_x &= \overline{V}_x e^{j(Z-1)\pi/3} - \overline{V}_1\\ \overline{V}'_y &= \overline{V}_y e^{j(Z-1)\pi/3} - \overline{V}_1\\ \overline{V}'_z &= \overline{V}_z e^{j(Z-1)\pi/3} - \overline{V}_1 \qquad (3)\end{aligned}$$

The fictitious vectors are similar to those of two level inverters.

TABLE II
PIVOT VECTORS AND INVERTER STATES

Sector Z	Pivot Vector $\overline{V}_z$	$\overline{V}_{zx}$	$\overline{V}_{zy}$
1	$\overline{V}_1$	100	0-1-1
2	$\overline{V}_2$	00-1	110
3	$\overline{V}_3$	010	-10-1
4	$\overline{V}_4$	-100	011
5	$\overline{V}_5$	001	-1-10
6	$\overline{V}_6$	0-10	101

The vector $V_z^{'}$ forms the origin and its magnitude is always
zero and for a given sector this vector is similar to the zero vector of two level inverters. The three nearest vectors can be identified as V_x, V_y, andV_z as shown in Fig. 3. Now the solution to (1)is similar to that of two level inverters, as in (4)

$$V'_{r\alpha}T_s = V'_{x\alpha}T_x + V'_{y\alpha}T_y \qquad (4a)$$
$$V'_{r\beta}T_s = V'_{x\beta}T_x + V'_{y\beta}T_y \qquad (4b)$$
$$T_z = T_s - T_x - T_y. \qquad (4c)$$

Thus, the computational complexity of three level inverters isreduced to that of two level inverters. Implementation of above method is simple as it requires only the computation Vr'of and is explained in Section IV.With the sector definition given above, all the sectors are symmetric and a modular approach can be used in implementation.

Conventional SVPWM sequences will have switching sequences $\overline{V}_{zx} \Leftrightarrow \overline{V}_z \Leftrightarrow \overline{V}_y \Leftrightarrow \overline{V}_{zy}$ .The T_z intervals equally derived between pivot vectors $\overline{V}_{zx}$ and $\overline{V}_{zy}$. The pivot vectors and are defined in Table II. V_{zx} State is defined as the state of V_z obtained by switching only one phase of the inverter from state . Similarly state $\overline{V}_{zy}$ is defined as The state of obtained by switching only one phase of the inverter from V_x state . These sequences ensure that in each sampling interval, each of the phases is switched at least once.Also these sequences satisfy following two conditions forminimum switching frequency.

- Condition 1: Only one switch is switched during state transition.That is transition from state 1 to state and vice versa is not allowed.
- Condition 2: The final state of present sample will be the initial state of next sample.

In the next section, these SVPWM sequences are modified to
achieve synchronized output waveforms with HWS and TPS. In the present method, the sector decides the angle through which the reference vector $\overline{V}_r$ is to be rotated to get the fictitiousreference vector $\overline{V}'_r$whereas

in the simplified method given in [7], the offset values to be subtracted $\overline{V}_r$ from to obtain $\overline{V}_r'$ has to be stored in the form of lookup table or programmed accordingly. This slight modification helps in developing subroutines to generate switching sequence and helps in implementing in DSP assembly program which is clear from the implementation details given in Section IV.

III. SPACE VECTOR APPROACH TO SYNCHRONIZATION AND SYMMETRY

In this section, the principles of obtaining synchronization
and various symmetry in terms of space vectors is derived.

A. Need for Synchronization and Symmetry

• Synchronization: At low switching frequencies, it is necessaryto maintain perfect synchronization of inverter outputvoltage with respect to its own fundamental to avoid sub-harmonics.This is possible if and only if the PWM outputpole voltage waveform satisfies the condition given below

$$v_{Rm}(\theta \pm 2\pi) = v_{Rm}(\theta)$$
$$v_{Ym}(\theta \pm 2\pi) = v_{Ym}(\theta)$$
$$v_{Bm}(\theta \pm 2\pi) = v_{Bm}(\theta)$$

where is θ any arbitrary angle measured from the reference axis. This can be achieved if the same inverter stateis switched at θ and $(\theta \pm 2\pi)$ and the dwell time of thesestates must be equal. This demands $\overline{V}_r$ the to be sampled at and $(\theta \pm 2\pi)$,which is possible only if there are integral number of samples per cycle of the fundamental.

• TPS: At low switching frequency, lower order harmonics are dominant. The PWM sequences should be designed to eliminate some of these harmonics. The three-phase symmetry will ensure that all the harmonics and the fundamental of all the three phases will be perfectly balanced. So the triplen harmonics will be cancelled from the line voltage. For a phase sequence of *R-Y-B*, the TPS can be achieved if the inverter output voltages of three phases satisfythe following condition:

$$v_{Bm}\left(\theta - \frac{2\pi}{3}\right) = v_{Ym}\left(\theta + \frac{2\pi}{3}\right) = v_{Rm}(\theta).$$

The above condition can be met if the switch position of pole R at θ , the switch position of pole Y at $(\theta+2\pi/3)$, and the switch position of pole ***B*** at $(\theta-2\pi/3)$ are same. For example, if the inverter state at $(\theta+2\pi/3)$ is (101), then at $(\theta-2\pi/3)$ the state (110) must be used and at state (011) must be used to achieve TPS and dwell time of these states must be equal.

• HWS: The half wave symmetry will ensure elimination of even harmonics from the output voltage. In order to achieve HWS, the pole voltage θ at $(\pi+\theta)$ and should have opposite polarity that is

$$v_{Rm}(\theta \pm \pi) = -v_{Rm}(\theta)$$
$$v_{Ym}(\theta \pm \pi) = -v_{Ym}(\theta)$$
$$v_{Bm}(\theta \pm \pi) = -v_{Bm}(\theta).$$

In order to achieve this, the switch position of a given phase
θ at $(\theta \pm \pi)$ and must be opposite. If at the switch position of a given phase is "1," then at $(\theta \pm \pi)$ it must be " -1" and
vice versa. But if the switch position of a given phase is
"0" at , then the switch position of the same phase must
be "0" at $(\theta \pm \pi)$.
The conditions of waveform symmetry for a given sample k are summarized in Table III. The necessary and sufficient conditions in terms of the inverter states to achieve synchronization

TABLE III
CONDITIONS OF SYNCHRONIZATION, HWS, AND TPS IN TERMS OF POLE VOLTAGES

	Synchronization	HWS	TPS	TPS
Pole voltage at θ	Pole voltage at $\theta \pm 2\pi$	Pole voltage at $\theta \pm \pi$	Pole voltage at $\theta + 2\pi/3$	Pole voltage at $\theta - 2\pi/3$
v_{Rm}	v_{Rm}	$-v_{Rm}$	v_{Bm}	v_{Ym}
v_{Ym}	v_{Ym}	$-v_{Ym}$	v_{Rm}	v_{Bm}
v_{Bm}	v_{Bm}	$-v_{Bm}$	v_{Ym}	v_{Rm}

TABLE IV
CONDITIONS OF SYNCHRONIZATION, HWS, AND TPS IN TERMS OF INVERTER STATES

	Synchronization	HWS	TPS	TPS
Inverter state at θ	Inverter state at $\theta \pm 2\pi$	Inverter state at $\theta \pm \pi$	Inverter state at $\theta + 2\pi/3$	Inverter state at $\theta - 2\pi/3$
S_R	S_R	S_R'	S_B	S_Y
S_Y	S_Y	S_Y'	S_R	S_B
S_B	S_B	S_B'	S_Y	S_R

and symmetry at the line and pole voltages are given in Table IV. In Tables III and IV, the states with a prime (') indicate the complementary states. Complementary state of 1 is -1state and vice versa and complementary state of 0 is state 0 itself. The conditions of HWS and TPS given in column 2 and 3 of Table IV, relate the inverter states over an interval of 60 . So the inverter states of each sector are related by (5)

$$S_R\left(\theta + \frac{\pi}{3}\right) = S_Y'(\theta)$$
$$S_Y\left(\theta + \frac{\pi}{3}\right) = S_B'(\theta)$$
$$S_B\left(\theta + \frac{\pi}{3}\right) = S_R'(\theta). \quad (5)$$

So one of the requirements of synchronization and symmetry is that, there should be integral number of samples (***N***) per sector and these samples should be placed at identical positions in each sector. Under these conditions, the sampled reference voltages satisfy the conditions given in Table IV. Hence, for a given sample , where $n = 1,2,3 \ldots N$ the dwell times

T_x, T_y and T_z of nearest three vectors will be equal in all the sectors.

B. Number of Samples per Sector, Pulse Number and Switching Sequence

*1) Odd Values of **N** :*For odd values of ***N***, there will be samples ***(N-1)*** within the sector placed at an equal distance of $(\pi/3N)$ and one sample on the sector boundary. Depending on how the change of $\overline{V}_z$ is accomplished, there are two possibilities.

• TYPE 1: All the samples except the sample on sector boundary will have sequences $\overline{V}_{zx} \iff \overline{V}_x \iff \overline{V}_y \iff \overline{V}_{zy}$.

The sample n=N which falls on the sector boundary willhave the sequence, $\overline{V}_{zx} \longrightarrow \overline{V}_x \longrightarrow \overline{V}_y$. The last state $\overline{V}_y$, of the ***N***thsample of the present sector will be the starting state $\overline{V}_{zx}$,in the first sample of the next sector. So the sample n=1will have $\overline{V}_{zx} \longrightarrow \overline{V}_x \longrightarrow \overline{V}_y \longrightarrow \overline{V}_{zy}$the sequence, .There will not be any switching from one sample to another sample during sector change over. The pulse number is given by ***P=(3/2)(N-1)***.

• TYPE 2: All the samples will have sequences $\overline{V}_{zx} \iff$.
$\overline{V}_x \iff \overline{V}_y \iff \overline{V}_{zy}$

The sequence of the last sample in a sector will always endwith state $\overline{V}_{zy}$and the first sample in a sector will start with $\overline{V}_{zx}$state . This type of sequences will cause an additionalswitching during sector change over. The pulse number is given by **P=(3/2)(N+1).**

*2) Even Values of :*For even values of N , all the sampleswill be within the sector placed at an equal distance of(π/3N) .All the samples except n=1 and n=Nwill have sequences
$\overline{V}_{zx} \iff \overline{V}_x \iff \overline{V}_y \iff \overline{V}_{zy}$.

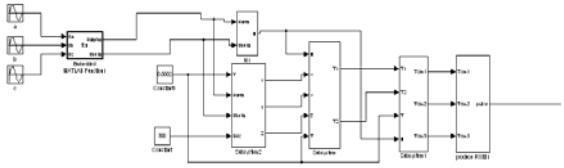
The sample n=1 and n=N will have the sequences $\overline{V}_{zx} \longrightarrow \overline{V}_x \longrightarrow \overline{V}_y \longrightarrow \overline{V}_x$ and $\overline{V}_x \longrightarrow \overline{V}_y \longrightarrow \overline{V}_x \longrightarrow \overline{V}_{zx}$.

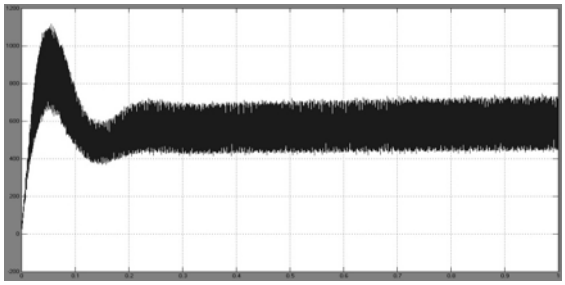
In these samples, one of the phases will be switched twiceand another phase will be clamped. The pulse number will be P=3N/2. Combining all the three cases, it can be seen thatsynchronization, HWS and TPS can be achieved for any integral value of***P*** .

It can be seen that these sequences also exhibit the conditions
of QWS given in (6) in addition to the conditions of synchronization, HWS and TPS, even though the sequences are designedwithout considering conditions of QWS

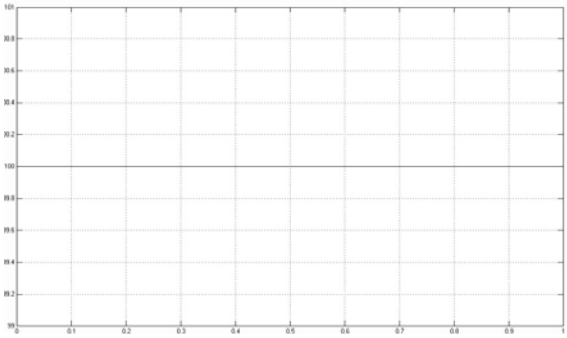
IV. SIMULATIONAND RESULTS

In this section the performance of Three level VSI is analyzedbased on different parameters using the system level simulationmade using MATLAB/SIMULINK software. Here the input sources are Wind and solar energies .the output of the wind renewable energy source show in fig5 .the out put of wind power supply is 630 V it's showing .Fig 6 shows supply from the solar panels of 100 DC .Fig. 4, represents the simulation model for the generationof PWM pulses for Three level VSI by using MSVPWM technique. In thismethod the reference voltage is located between two voltagevectors V_i and V_{i+1}. Time period for all states varies with thevoltage sector. The voltage vector is then compared with rampsignal. Based on the angle of the rotating reference voltage inthe six voltage space vector the pulses are generated.2



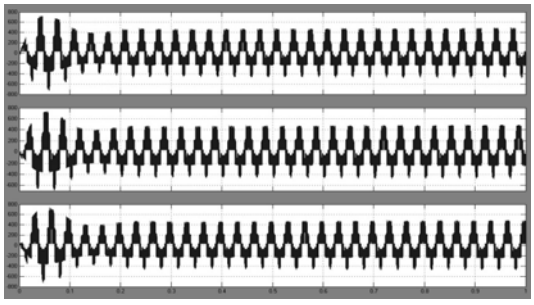


Wind power supply of 630V



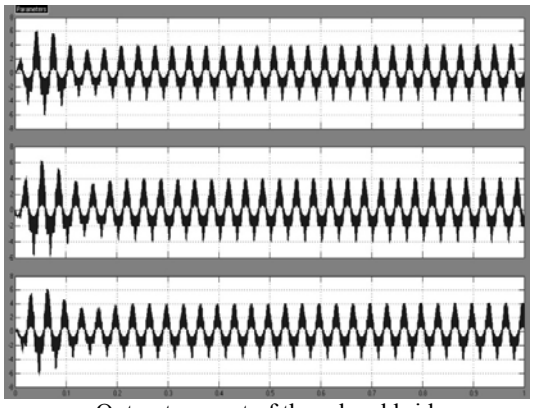
Solar power supply of 100V

In above simulation the modified SVPWM is shown ,in this for 100 reference voltage the 3 level voltages shown ,Udc=300,time signal as 0.0002 .

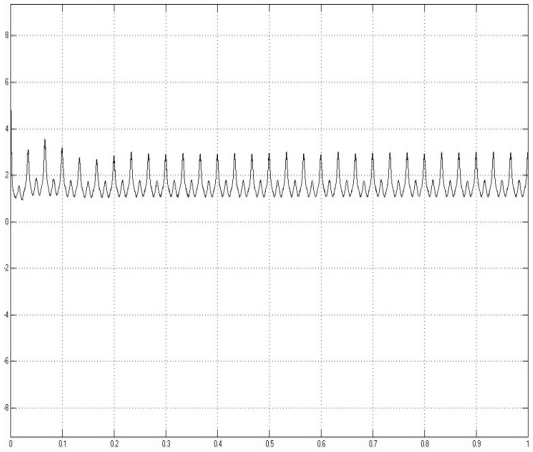


Out put voltages of three level bridge
Out put currents

Total harmonic distortions are shown in circuit varying0.5 to 3 the harmonic distortion is very less compared to conventional space vector pulse width modulation.



Out put current of three level bridge



Total harmonic distortion

CONCLUSION

The theory of the space vector based synchronized PWM method with HWS and TPS is explained. The experimental results are presented. The proposed model is simple to implement on digital controllers and does not add to any computational complexity. It is shown that V_{WTHD} the proposed PWM technique will result in balanced dc link capacitor voltages. The performance results show that of the proposed method is better compared to that of synchronized SPWM technique and synchronized SVPWM technique without symmetries. The simulation waveforms show HWS and TPS for any integer value of pulse number. The absence of triplen harmonics from the line voltage shows that the inverter output voltages have three phase symmetry. Even though the focus is on low switchingfrequency applications, the proposed technique can be used for high switching frequency applications also.

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INCREASE IN SPEED AND REDUCING POWER BASED ON SHIFT-AND-ADD ARCHITECTURE THROUGH BZ-FAD: BY PASS ZERO FEED A DIRECTLY

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Abstract—In this paper, a low-power structure called bypass zero, feed A directly (BZ-FAD) for shift-and-add multipliers is proposed. The architec-ture considerably lowers the switching activity of conventional multipliers. The modifications to the multiplier which multiplies A by B nclude the removal of the shifting the B register, direct feeding of A to the adder, bypassing the adder whenever possible, using a ring counter instead of a binary counter and removal of the partial product shift. The architecture makes use of a low-power ring counter proposed in this work. Simulation results for 32-bit radix-2 multipliers show that the BZ-FAD architecture lowers the total switching activity up to 76% and power consumption up to 30% when compared to the conventional architecture. The proposed mul-tiplier can be used for low-power applications where the speed is not a pri-mary design parameter.

Keywords— Hot-block ring counter, low-power multiplier, low-power ring counter, shift-and-add multiplier, switching activity reduction.

I. INTRODUCTION

Multipliers are among the fundamental components of many digital systems and, hence, their power dissipation and speed are of prime concern. For portable applications where the power consumption is the most important parameter, one should reduce the power dissipation as much as possible. One of the best ways to reduce the dynamic power dissipation, henceforth referred to as power dissipation in this paper, is to minimize the total switching activity, i.e., the total number of signal transitions of the system. In Very Large Scale Integration, Low power VLSI design is necessary to meet MOORE'S law and to produce consumer electronics with more back up and les weight. Multiplication occurs frequently in finite impulse response filters, fast Fourier transforms, discrete cosine transforms, convolution, and other important DSP and multimedia kernels. The objective of a good multiplier is to provide a physically compact, good speed and low power consuming chip. Many research efforts have been devoted to reducing the power dis-sipation of different multipliers (e.g., [1]–[3]). The largest contribu-tion to the total power consumption in a multiplier is due to genera-tion of partial product. Among multipliers, tree multipliers are used in high speed applications such as filters, but these require large area. The carry-select-adder (CSA)-based radix multipliers, which have lower area overhead, employ a greater number of active transistors for the multiplication operation and hence consume more power. Among other multipliers, shift-and-add multipliers have been used in many other ap-plications for their simplicity and relatively small area requirement [4]. Higher-radix multipliers are faster but consume more power since they employ wider registers, and require more silicon area due to their more complex logic. In this work, we propose modifications to the conventional architec-ture of the shift-and-add radix-2 multipliers to considerably reduce its energy consumption. This paper is organized as follows: toward a low power shift-and-add multiplier (see Section II), hot block ring counter (see Section III), results and discussion in Section IV with Section V containing summary.

II. TOWARD A LOW POWER SHIFT-AND-ADD MULTIPLIER

A. Main Sources of Switching Activity

The architecture of a conventional shift-and-add multiplier, which multiplies by is shown in Fig. 1 [4]. There are six major sources of switching activity in the multiplier. These sources, which are marked with dashed ovals in the figure, are: (a) shifts of the B register;(b) activity in the counter; (c) activity in the adder; (d) switching between "0" and A in the multiplexer; (e) activity in the mux-select controlled by B(0); and (f) shifts of the partial product (PP) register.Note that the activity of the adder consists of required transitions(when B(0) is nonzero) and unnecessary transitions (when B(0) is zero).

By removing or minimizing any of these switching activity source one can lower the power consumption. Since some of the nodes have higher capacitance, reducing their switching will lead to more power reduction. As an example, 333 is the selector line of the multiplexer which is connected to ß gates for a ß-bit multiplier. If we somehow eliminate this node, a noticeable power saving can be achieved. Next, we describe how we minimize or possibly eliminate

these sources of switching activity.

B. Proposed Low Power Multiplier: BZ-FAD

To derive a low-power architecture, we concentrate our effort on eliminating or reducing the sources of the switching activity discussed in the previous section. The proposed architecture which is shown in Fig. 2 is called BZ-FAD

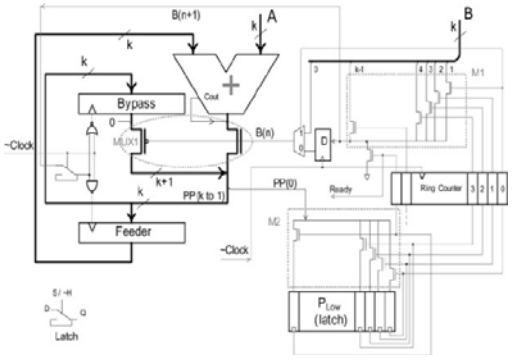


Fig. 2. Proposed low power multiplier architecture (BZ-FAD).

a) Shift of the B Register: In the traditional architecture (see Fig. 1), to generate the partial product, B(0) is used to decide between A and 0. If the bit is "1", A should be added to the previous partial product, whereas if it is "0", no addition operation is needed to generate the partial product. Hence, in each cycle, register should be shifted to the right so that its right bit appears at B(0); this operation gives rise to some switching activity.To avoid this, in the proposed architecture (see Fig. 2) a multiplexer (M1) with one-hot encoded bus selector chooses the hot bit of B in each cycle. A ring counter is used to select B(n) in the nth cycle. As will be seen later, the same counter can be used for block M2 as well. The ring counter used in the proposed multiplier is noticeably wider (32 bits versus 5 bits for a 32-bit multiplier) than the binary counter used in the conventional architecture; therefore an ordinary ring counter, if used in BZ-FAD, would raise more transitionsthan its binary counterpart in the conventional architecture. To minimize the switching activity of the counter, we utilize the low-power ring counter, which is described in Section 2-B2.

b) Reducing Switching Activity of the Adder: In the conventional multiplier architecture (see Fig. 1), in each cycle, the current partial product is added to A (when B(1) is one) or to 0 (when B(0) is zero).This leadsto unnecessary transitions in the adder when B(0) is zero. In these cases, the adder can be bypassed and the partial productshould be shifted to the right by one bit. This is what is performed in the proposed architecture which eliminates unnecessary switching activities in the adder. As shown in Fig. 2, the Feeder and Bypass registers are used to bypass the adder in the cycles where B(n) is zero. In each cycle, the hot bit of the next cycle (i.e., B(n+1)) is checked. If it is 0, i.e., the adder is not needed in the next cycle, the Bypass register is clocked to store the current partial product. If B(n+1) is 1, i.e., the adder is really needed in the next cycle, the Feeder register is clocked to store the current partial product which must be fed to the adder in the next cycle. Note that to select between the Feeder and Bypass registers we have used NAND and NOR gates which are inverting logic, therefore, the inverted clock (Clock in Fig. 2) is fed to them. Finally, in each cycle, B(n) determines if the partial product should come from the Bypass register or from the Adder output.

In each cycle, when the hot bit B(n) is zero, there is no transition in the adder since its inputs do not change. The reason is that in the previous cycle, the partial product has been stored in the Bypassregister and the value of the Feeder register, which is the input of the adder, remains unchanged. The other input of the adder is A, which is constant during the multiplication. This enables us to remove the multiplexer and feed input A directly to the adder, resulting in a noticeable power saving. Finally, note that the BZ-FAD architecture does not put any constraint on the adder type. In this work, we have used the ripple adder which has the least average transition per addition among the look ahead, carry skip, carry-select, and conditional sum adders [5].

c) Shift of the PP Register: In the conventional architecture, the partial roduct is shifted in each cycle giving rise to transitions. Inspecting the multiplication algorithm reveals that the multiplication may be completed by processing the most significant bits of the partial product, and hence, it is not necessary for the leastsignificant bits of the partial product to be shifted. We take advantage of this observation in the BZ-FAD architecture. Notice that in Fig. 2 for P_{ixo} , the lower half of the partial product, we use k latches (for a k-bit multiplier). These latches are indicated by the dotted rectangle P_{ixo} in Fig. 2. In the first cycle, the least significant bit PP(0) of the product becomes finalized and is stored in the right-most latch of P_{ixo} . The ring counter output is used to open (unlatch) the proper latch. This is achieved by connecting the S/~H line of the nth latch to the nth bit of the ring counter which is "1" in the nth cycle. In this way, the nth latch samples the value of the nth bit of the final product (see Fig. 2). In the subsequent cycles, the next least significant bits are finalized and stored in the proper latches.

When the last bit is stored in the left-most latch, the higher and lower halves of the partial product form the final product result.Using this method, no shifting of the lower half of the partial product is required. The higher part of the partial product, however, is still shifted. Comparing the two architectures, BZ-FAD saves power for two reasons: first, the lower half of the partial product is not shifted, and second, this half is implemented with latches instead of flip-flops. Note that in the conventional architecture (see Fig. 1) the

data transparency problem of latches prohibits us from using latches instead of flip-flops for forming the lower half of the partial product. This problem does not exist in BZ-FAD since the lower half is not formed by shifting the bits in a shift register. In brief, from the six sources of activity in the multiplier, we have eliminated the shift of the B register, reduced the activities of the right input of the adder, and lowered the activities on the multiplexer select line. In addition, we have minimized the activities in the adder, the activities in the counter, and the shifts in the PP (partial product) register.The proposed architecture, however, introduces new sources of activities. These include the activities of a new multiplexer which has the same size as that of the multiplexer of the conventional architecture. Note that the higher part of the partial product in both architectures has the same activity. As will be seen in Section 4 the net effect is a lower switching activity for BZ-FAD compared to that of the conventional multiplier.

III. HOT BLOCK RING COUNTER

In the proposed multiplier, we make use of a ring counter architecture of which is described in this section.

In a ring counter always a single "1" is moving from the right to the left. Therefore in each cycle only two flip-flops should be clocked. To reduce the switching activity of the counter, we propose to partition the counter into Ě blocks which are clock-gated with a special multiple-bit clock gating structure shown in Fig. 4, whose power and area overheads are independent of the block size. In the proposed counter, called *Hot Block* ring counter (see Fig. 3) fewer superfluous switching activity ex-ists and there are many flip-flops whose outputs do not go to any clock gating structure. This noticeably reduces the total switching activity of the ring counter.

We have utilized the property that in each cycle, the outputs of all flip-flops, except for one, are "0". Thus in the partitioned ring counter of Fig. 3, there is exactly one block that should be clocked (except for the case that the "1" leaves a block and enters another). We call this block the Hot Block. Therefore, for each block, the clock gating structure (CG) should only know whether the "1" has entered the block (from the right) and has not yet left it (from the left). The CG starts passing the clock pulses to the block once the "1" appears at the input of the first flip-flop of the block. It shuts off the clock pulses after the "1" leaves the left-most flip-flop of theblock.

Fig. 3. Hot Block architecture for a 16-bit ring counter—

The ring counter is partitioned into Ě blocks of size˜ ˜(is 4 in this figure). Only two clock gators are shown.

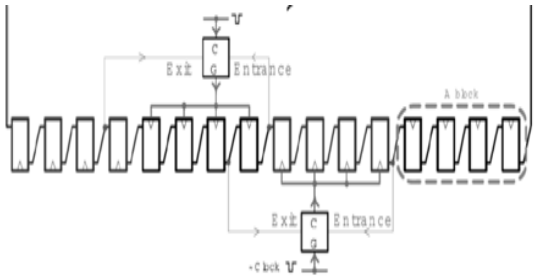
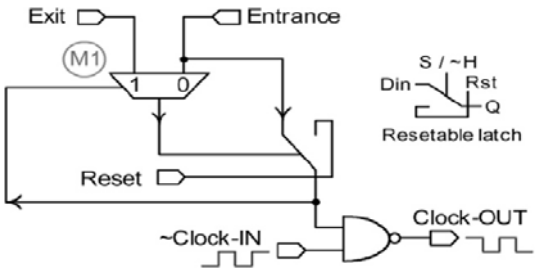


Fig. 4. Clock gating structure used in the proposed architecture



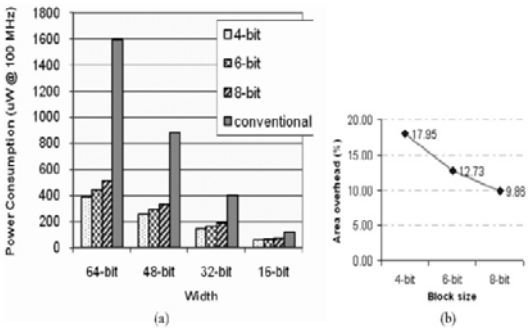


Fig. 5. (a) Power consumption of the conventional ring counter versus that of the Hot-Block ring counter with different block sizes. (b) The area overhead for different block sizes.

The clock gating structure (CG) proposed for the Hot Block ring counter is shown in Fig. 4. It is composed of a multiplexer ₃₃, a NAND gate, and a resettable latch. In this work, the multiplexers are implemented with transmission gates. In addition to the *Reset* and ₃ ₃☼ ß 0 ₃β signals, there are two other signals called *Entrance* and *Exit*, coming from the neighboring left and right blocks. These are used to determine whether the "1" is present in the block to which the output of the CG goes. When the active high Reset signal is "1", the latch is reset which causes the value of the Entrance signal to be placed on the ₃₃ ₃ ₃ line of the latch through multiplexer M1. This in turn causes the latch to read the *Entrance* signal, which was previously reset to "0", since the

whole ring counter is reset and all the bits except the first are reset to "0". After a sufficiently long interval, *Reset* goes to "0" and since *Entrance* has a value of "0", the latch keeps holding "0" on its output, forcing *Clock-OUT* to "1" after the CG is reset. This condition should persist until the "1" is about to enter to the block.

Multiplexer ₃₃ plays the watchdog role. After the CG is reset the selector line of multiplexer ₃₃, has the value of "0" which causes the *Entrance* signal to be selected (watch dogged) by this multiplexer. The output of the latch is also connected to the NAND gate which causes the input clock signal to be shut off (gated), after the CG is reset. The *Entrance* and *Exit* signals have special meanings as follows. When "1", *Entrance* means that the "1" is about to enter the block in the next cycle. This line is connected to the block input, namely, the input of the right-most flip-flop in the block, as shown in Fig. 3. The *Exit* signal on the other hand indicates the "1" has left the block and hence it should no longer be clocked. Notice that the *Exit* signal is connected to the output of the right-most flip-flop of the left hand block (see Fig. 3).

Once the *Entrance* signal becomes "1", the sample and data-in lines of the latch are set to "1". This causes multiplexer ₃₃ to select (watch dog) the *Exit* signal which is "0", since all cells of the ring counter ex-cept one, have the value of "0" in them. Through multiplexer ₃₃, the value of the Exit signal ("0") goes to the ₃₃ ₃ ₃ line of the latch, which in turn causes the latch to hold "1" (the value of the *Entrance* signal) on its output. From this moment on, the *Exit* signal is watch dogged by multiplexer ₃₃; in addition, clock pulses are no longer gated by the NAND gate. To reduce the layout area, we have used a NAND gate instead of an AND gate, and thus, the input clock signal to the clock gator should be the inverted clock (₃ ₃☼₃ ß 0 ₃β in Fig. 4). In the cycles when the *Entrance* signal becomes "1", no positive clock edges should appear at the output of the clock gator; instead it should only prepare to pass clock pulses during the next clock cycles. This is achieved by using the inverted clock signal; the flip-flops are pos-itive-edge triggered, and hence, when the *Entrance* signal, which is the output of some flip-flop, becomes "1" at a positive clock edge, the ₃ ₃☼ ß 0 ₃β (see Fig. 4) is "0" (negative edge), meaning that no extra positive edge is produced at the clock gator output.

The clock pulses come to the clock gating structure, propagate through the NAND gate, and go to the block cells via *Clock-OUT*, until the *Exit* signal becomes "1". Then the ₃₃ ₃ ₃ line of the latch becomes "1" through multiplexer ₃₃ causing the latch to read its input (the *Entrance* signal), which is '0' at this time. The "0" prop-agates through the latch and reaches the selector line of multiplexer ₃₃ giving rise to the *Entrance* signal to be watch dogged again. The output of the latch, which is "0" in this state, also forces the NAND gate to shut off the input clock pulses. Note that regardless of the block size, the proposed CG (see Fig. 4) has a total of four inputs.

IV. RESULTS AND DISCUSSION

In this section, we present experimental results for the proposed ring counter and multiplier. We used Synopsys Design Compiler for the synthesis and Synopsys Prime Power for the power simulation with the TSMC 0.13-₃m CMOS technology. Since we have used a standard cell library for this technology, all pass-transistors have been replaced with buffers during the synthesis of the implementations.

V. RELATED WORKS OF EACH BLOCK IN THE PROPOSED SYSTEM

A. RING COUNTER

In Fig. 5(a), you can see the power consumption of the conventional and Hot Block (see Fig. 3) ring counters of 16-, 32-, 48-, and 64- bits. As seen in this diagram, the efficiency of the Hot Block architecture is more pronounced as the width of the ring counter increases; e.g., with the width of 64 bits, the conventional and Hot-Block consume 1591 and 389 ₃W, respectively. The maximum power reduction is achieved for a 64-bit ring counter with blocks of 4 flip-flops, where a power reduction of 75% is achieved.

Now, we estimate the area overhead of the proposed ring counter. Note that the hot block clock gating structure (see Fig. 4) can be imple-mented using 18 transistors, which include 10 for the resettable latch, 4 for the multiplexer, and 4 for the NAND gate. As mentioned earlier, the multiplexers were implemented with transmission gates. Each flip-flop needs 18 transistors and hence for a block size of ₃ (₃ flip-flops) the

TABLE I
COMPARISON OF THE TRANSITION COUNTS OF THE BZ-FAD
(WHEN APPLYING A SUBSET WITH 100 OPERAND PAIRS)

Component	BZ-FAD	Conventional	Reduction (%)
Low order partial product	6,564 (latch)	82,208 (Register *B*)	92.02 %
Adder	46,301	74,870	38.16 %
Multiplexer	56,722	10,013 (mux *A*)	-82.35 %
Counter	20,965	22,937	8.60 %

area overhead of the hot block clock gating structure, in terms of the number of transistors.

The area overhead Fig. 5(b) is dependent on the block size such that as the block size increases the area overhead decreases. However, the larger the block size is, the higher the power consumption is.The critical path of the Hot Block architecture is the same as that of the conventional architecture except that the clock signal in the Hot Block passes through a NAND gate (see Fig. 4). Therefore, the edge difference between the ——————————— and Clock-OUT, which is independent of the counter width, is equal to the delay of a NAND gate.This technology dependent delay is very short (e.g., about 10 ps for the TSMC 0.13-———————————————m CMOS).

B. MULTIPLIER

To evaluate the efficiency of the proposed architecture, we implemented three different Radix-2 16-bit multipliers corresponding to the conventional, BZ-FAD and SPST architectures. The spurious power suppression technique (SPST) architecture is a very low-power treebased array multiplier published recently in the literature [6]. In general, array multipliers offer high speed and low power consumption. However they occupy a lot of silicon area. The SPST results presented in this paper are based on our implementation of this multiplier and are in agreement with the authors' published results. For SPST implementation we used the circuit details of [6]–[8]. To determine the effectiveness of the power reduction techniques discussed in Section II, we have reported in Table I the switching activities of major common blocks of the BZ-FAD and conventional multipliers. As an example, the adder in BZ-FAD has 38.16% less switching activity compared to that of the conventional architecture. The higher switching activity of the BZ-FAD multiplexer is due to its higher fan-out. As another comparison, the power consumption of the multipliers for normally distributed input data are reported in Figs. 6 and 7. As seen in Fig. 6, the BZ-FAD multiplier consumes 30% lower power compared to the conventional multiplier. The BZ-FAD multiplier has about 34% area overhead.

In Fig. 7, the area overhead and the power reduction of the BZ-FAD multiplier are compared with those of the SPST multiplier. As seen in the figure, the power saving of SPST is slightly (about 6%) higher than that of BZ-FAD while its area is considerably larger (about 5 times). Finally, in Table II, we have compared the BZ-FAD multiplier with some other published low-power multipliers (excerpted from [6]). The results reveal that the BZ-FAD multiplier may be considered as a very low-power, yet highly area efficient multiplier. In terms of the area, the proposed technique has some area over head compared to the conventional shift-and-add multiplier. Compar-ison between Figs. 1 and 2 reveals that $_{33}$, $_{33}$, and the ring counter are responsible for additional area in the proposed architecture. The area overheads of the ring counter and multiplexers $_{33}$ and $_{33}$ scale.

Fig. 6. Comparison of the multipliers in terms of (a) power consumption and(b) area.

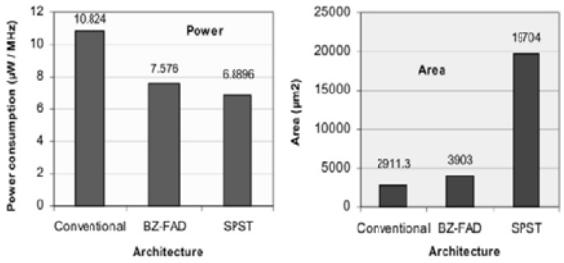


Fig. 7. Power reduction and area overhead of BZ-FAD and SPST [6] in com-parison with the conventional shift-and-add multiplier

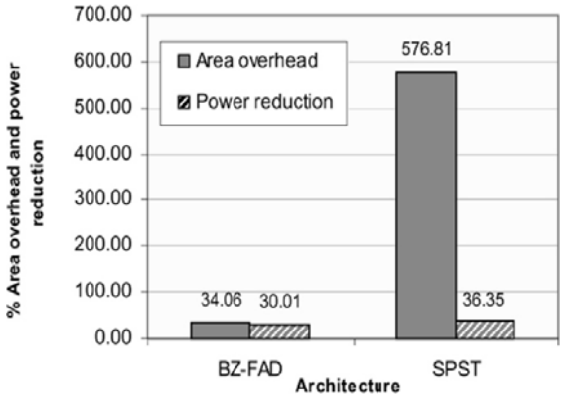


TABLE II

COMPARISON OF DIFFERENT MULTIPLIERS FOR NORMALLY DISTRIBUTED RANDOM DATA IN TERMS OF ENERGY PER MULTIPLICATION

Multiplier	Width	Technology	Energy (pJ)	Area
Wang [9]	32-bit	0.35μ	798.6	19,743 (gates)
Chen [10]	16-bit	0.25μ	346	0.337 (mm^2)
Huang [11]	32-bit	0.18μ	406.5	74,598 (tr.)
Lee [12]	4, 8, 16-bit	0.13μ	52	6,388 (gates)
SPST [6]	16-bit	0.13μ	42	11,028 (tr.)
BZ-FAD	16-bit	0.13μ	48.5	3,903 (μm^2)
Conventional	16-bit	0.13μ	69.2	2,911 (μm^2)

up linearly with the input data width. This leads to a small increase in the leakage power which, as the results reveal, is less than the overall power reduction. The leakage power of the 16-bit BZ-FAD architec-ture is about 11% more than that of the conventional architecture but the contribution of the

leakage power in these multipliers is less than 3% of the total power for the technology used in this work. Finally, note that since the critical paths for both architectures are the same (see Section IV-C), neither of the two architectures has a speed advantage over the other.

C. CRITICAL PATH ANALYSIS

By comparing the two architectures, it is observed that in BZ-FAD, the value of does not contribute to the critical path whereas in the conventional multiplier, it should first settle since ₃₃ is required for the multiplexer to select either ğ or zero. In BZ-FAD, "ğ" has al-ready settled and only the output of the *Feeder* register which is the other input to the adder needs to settle. Next, we consider the BZ-FAD *MUX1*, whose select signal does not contribute to the critical path. This is because the adder in the BZ-FAD, in contrast to the conventional ar-chitecture, can begin its work independent of multiplexer *MUX1*. In fact, while the adder is busy with performing the addition, there is enough time for the ring counter and multiplexer ₃₃ to deliver the value of the next hot bit. All delays in this path are shorter than the adder delay and, hence, do not increase the delay of BZ-FAD. The syn-thesis timing reports estimates the critical path delay for the BZ-FAD and the conventional multipliers to be 9.76 and 9.74 ns, respectively, which agrees with the above discussion. The slight difference between the reported delays originates from the fact that the input clock signal to the *Feeder* and *Bypass* registers pass through a NAND and a NOR gate in the BZ-FAD architecture. For SPST (synthesized in gate level) the critical path is about 25 ns.

SUMMARY AND CONCLUSION

In this paper, a low-power architecture for shift-and-add multipliers was proposed. The modifications to the conventional architecture in-cluded the removal of the shift of the register (in ğ 2), direct feeding of ğ to the adder, bypassing the adder whenever possible, use of a ring counter instead of the binary counter, and removal of the par-tial product shift. The results showed an average power reduction of 30% by the proposed architecture. We also compared our multiplier with SPST [6], a low-power tree-based array multiplier. The compar-ison showed that the power saving of BZ-FAD was only 6% lower than that of SPST whereas the SPST area was five times higher than that of the BZ-FAD. Thus, for applications where small area and high speed are important concerns, BZ-FAD is an excellent choice. Additionally, we proposed a low-power architecture for ring coun-ters based on partitioning the counter into blocks of flip-flops clack gated with a special clock gating structure the complexity of which was independent of the block sizes. The simulation results showed that in comparison with the conventional architecture, the proposed archi-tecture reduced the power consumption more than 75% for the 64-bit counter.

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DESIGNING A 16 TRANSISTORS 4 TO 2 COMPRESSOR

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Abstract—Compressors are basic components in many applications such as producing partial sums in multiplying. In this paper a new high speed 4 to 2 compressor is presented using 16 transistors and without using a power supply in CMOS logic. Suggested circuit is compared to typical structures to show produced improvements. Mentioned structure insisted on using 3 transistors XOR and PTL 2 transistors multiplexers in building circuits which at last results in high speed and fascinating design. In mentioned structure, despite typical outputs, XOR and multiplexer outputs are used effectively to increase performance of the compressors.

Keywords-16 transistor 4 to 2 compressor, high speed, zero statical power consumption

I. INTRODUCTION

In many single goal microprocessors and digital signal processors, multiplying is one of the most important operations in digital processing units which depend on setting up the ALUs and floating point units for performing commands such as convolution and filtering. Basically, multiplying consists of 3 steps: first, partial products are produced using an improved encoding to reduce the number of partial products. Then by using compressor circuits which are combined to form Wallace tree, partial products' matrix are reduced to 2 rows. Finally, a 2 input adder is used to add two rows.

As seen clearly, the second phase which is the reduction of partial products has the most critical operation because it is affected by the performance and area of the multiplier. A compressor, in its simplest type, is a circuit which reduces 3 rows of partial products into 2 rows, thus is called 3 to 2 compressor. To increase the speed of compression, several high order compressors, called 7 to 2 and 5 to 2 compressors are presented [2-5].

In many installs, compressor is located in the critical circuit path, thus request for high speed low power compressors greatly increases [6-8]. This paper presents a new model of 4 to 2 compressor based on using 3 transistors XOR gates. Using these gates causes proper output usage of previous parts and performance improvements of the system. Also rather than these gates, a multiplexer is used to improve time speed in critical path [9].

II. 4 TO 2 COMPRESSORS

These compressors have 4 inputs X1, X2, X3, X4, two outputs; sum and carry and a carry-out bit which is shown in Fig.1. Cin input is the valid output of former and Cout is the output of very compressor which goes to the next floor.

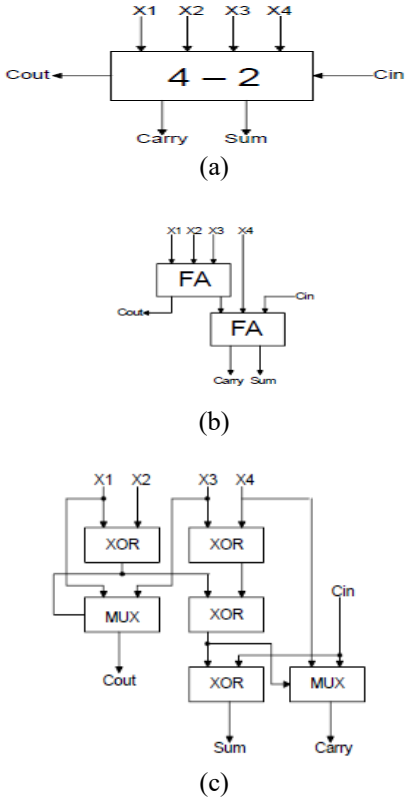


Fig.1 (a) a 4 to 2 compressor. (b) Standard implementation of a 4 to 2 compressor. (c) Conventional implementation of a 4 to 2 compressor.

Performance equation of 4 to 2 compressor is:

X1+X2+X3+X4+Cin=Sum+2*(Carry+Cout) (1)

Standard implementation of 4 to 2 compressor using 2 full adders is feasible which is shown in Fig 1.b. In Fig 1.c we can see the traditional implementation of this compressor. This compressor consists of 4 XOR gates, 2 inputs, two 2 to 1 MUX.

Equations for this compressor are:

Sum=X1⊕X2⊕X3⊕X4⊕Cin (2)

Cout=(X1⊕X2).X3+$\overline{(X1 \oplus X2)}$.X1 (3)

(4)

Carry=(X1⊕X2⊕X3⊕X4).Cin+
$\overline{(X1 \oplus X2 \oplus X3 \oplus X4)}$.X4

We can implement this compressor in MCML logic [10]. Diagram and circuit implementations can be seen in Fig 2. As seen, this circuit consists of 2 XOR gates and 2 carry producer unit of CGEN. In this architecture, output equations follow the same initial equations. As seen, beyond voltage supply, these circuits need a separate reference voltage. Another defect for this system is the need to 4 inverters for reversing all 4 inputs of the compressor which leads to increase in delay and number of transistors and power consumptions.

In the third architecture of this compressor, four 2 to 1 MUX and two XOR/XNOR gates are used [11]. Diagram of this architecture and circuit schematics of consisting components can be seen in Fig 3. Equations for outputs of 4 to 2 compressors are:

(5)

Sum=(X1⊕X2). $\overline{(X3 \oplus X4)}$ +
$\overline{(X1 \oplus X2)}$.(X3 ⊕X4).$\overline{(Cin)}$ +
$\overline{((X1 \oplus X2).\overline{(X3 \oplus X4)} + \overline{(X1 \oplus X2)}.(X3 \oplus X4))}$.Cin

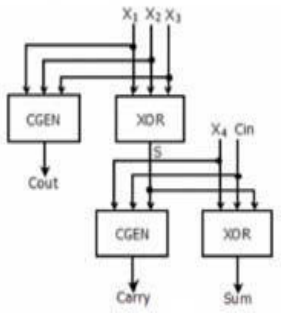
(6)

Cout=(X1 ⊕ X2).X3+
$\overline{(X1 \oplus X2)}$.X1

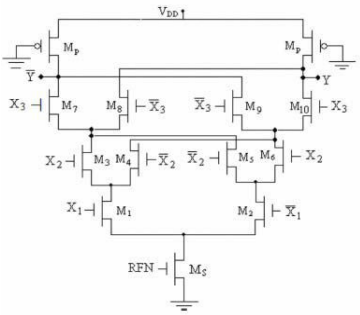
(7)

Carry=(X1⊕X2⊕X3 ⊕$\overline{X4}$).Cin +
$\overline{(X1 \oplus X2 \oplus X3 \oplus X4)}$.X4

As seen, Cout and carry are the same in first and third architecture and the difference between these two is only in sum equations. This circuit has better performance than traditional configurations.



(a)



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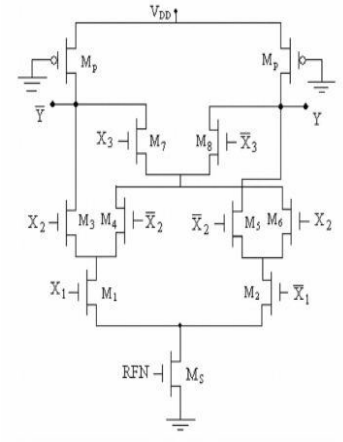
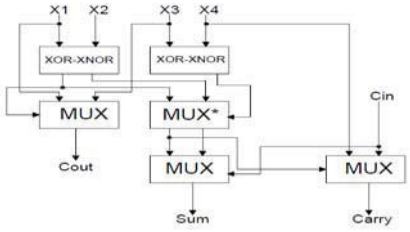
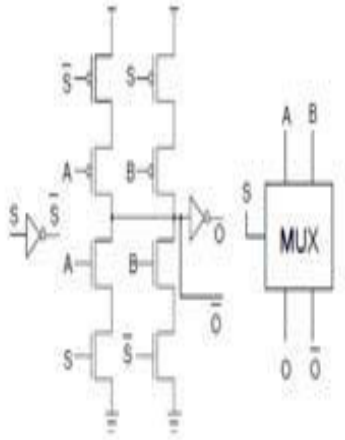


(c)

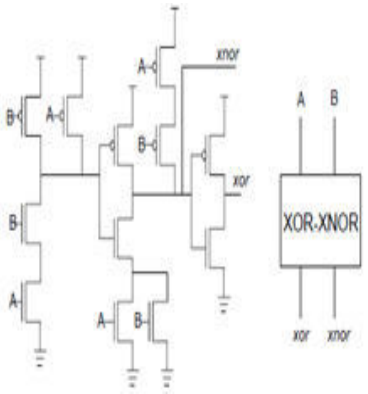
Fig. 2 (a) block diagram of the compressor in MCML (b) MCML(CGEN) carry producing circuit (c) MCML three input XOR/XNOR



(a)



(b)



(c)

Fig 3 (a) third architecture block diagram (b) MUX circuit (c) XOR/XNOR gate circuit in third architecture.

III. SUGGESTED CIRCUIT

Our main goal is building a 4 to 2 compressor by the least number of transistors in CMOS logic. What is clear is that compressor components often consist of MUX and XOR gate. As observed, we need to use a XOR gate in a 4 to 2 compressor. To configure presented gate in Fig 3c we need 12 transistors, so this causes increase in power consumption and occupied area on a silicon surface, thus this is not a proper circuit. By introducing PTL circuits a new approach was presented for electronic circuits and VLSI. In such circuits there was no power supply, thus static power reduced. On the other hand, by reducing the number of transistors, essential surface for configuration also decreases.

In figure 4 the circuit schematic of a 3 transistors XOR gate can be seen [12]. This circuit has no static power and occupies little area.

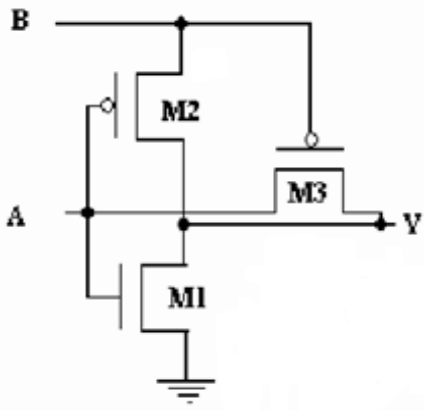


Fig4. 3 transistors XOR gate implementation.

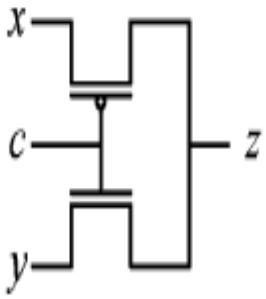


Fig 5. 2 transistors mux gate implementation.

By using this gate, in the architecture type 1, we can have the least number transistors.

It's notable that in a 12 transistors XOR gate, first, XNOR output is produced and then main output is produced by using an inverter. This causes increase in power consumption. This is also true for MUX, such that the final response is achieved by passing an inverter. Pay attention that the number of all unused outputs is decreased using outputs and their complement and finally the total power consumption and required number of transistors [13-15]. So our suggested compressor follows first architecture and consists of four 3 transistors XOR, and two transistors PTL MUX, as seen in Fig 5.

IV. SIMULATION AND RESULT ANALYSIS

Circuit simulation was done using HSPICE software with 180nm technology in the range of 0.9 to 3.3V and all the inputs were supplied by 100 MHz frequency.

In table 1, results of new circuit and configured previous samples in CMOS logic in 1.2 to 3.3 V are given.

The results indicate that output delay of new compressor in compared to the least time delay reference suggested circuits [11], [16] are improved by 64.16% and 92.77% respectively.

In fig. 6 we can see input pulses with different delays, so that conditions for different inputs are created. As seen, sum output is a bit weaker which is because of 3 XORs. As we know, we use PTL Mosfets for XORs and MUXs and these Mosfets show some voltage drop because of voltage drop on drain to source and they also have the weakest condition because sum has 3 XORs in its path.

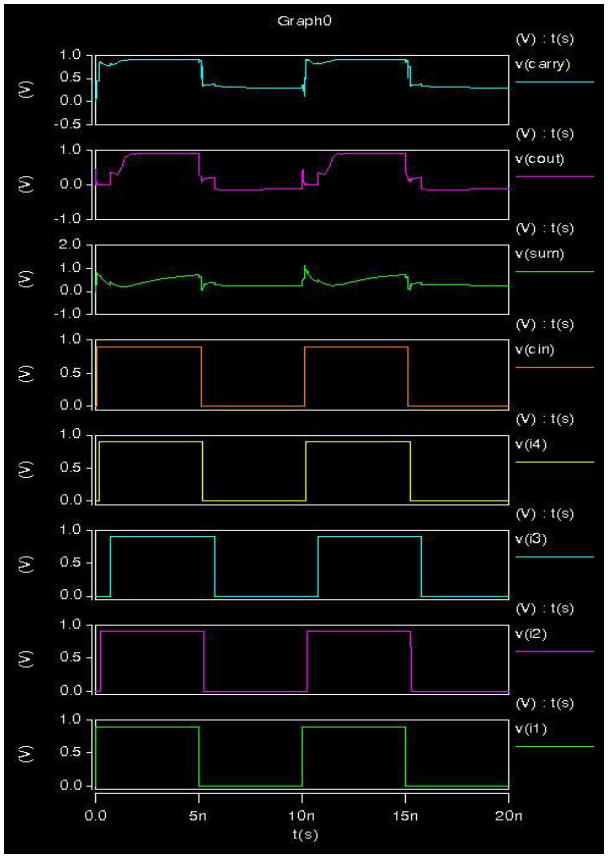


Fig 6. input and output diagram of 4 to 2 compressor .

Table 1.output delay (nS) for 4 to 2 comperessor.

	1.2	1.8	2.5	3.3
[11]	2.52	1.67	1.24	1.12
[16]	9.97	3.26	1.88	1.37
Suggested circuit	0.83	0.003	0.001	0.001

CONCLUSION

In this paper, a new 4 to 2 compressor in CMOS logic using 8 transistors is presented. New compressor has zero static power because of using no power supply. This compressor has a delay of 0.001ns for high voltage (voltage>1.5V) which is improved by 92% compared to its previous models.

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PERFORMANCE EVALUATION OF DS-CDMA RECEIVERS USING GENETIC ALGORITHM

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Abstract—Direct sequence-code division multiple access (DS-CDMA) technique is used in cellular systems where users in the cell are separated from each other with their unique spreading codes. These systems suffer from multiple access interference (MAI) due to other users transmitting in the cell, channel inter symbol interference (ISI) due to multipath nature of channels in presence of additive white Gaussian noise (AWGN).
This paper presents an investigation on use of new type of DSCDMA receiver called Genetic Algorithm based DS-CDMA receiver. Genetic Algorithm is robust optimization technique and does not fall into local minima, hence this gives better weight optimization of any system.
Extensive simulation studies demonstrate the performance of the different linear and nonlinear DS-CDMA receivers like RAKE receiver, matched filter (MF) receiver, minimum mean square error (MMSE) receiver using gold sequences and the performance has been compared with GA based receiver. It is seen that GA based DS-CDMA receiver performs much better than other type of receivers.

Keywords-DS-CDMA, genetic algorithm-based multi-user detector.

I. INTRODUCTION

Spread spectrum techniques have been wildly used in wired and wireless communications. The spreading of the signal spectrum gives us many advantages such as robustness against interference and noise, low probability of intercept, realization of Code Division Multiple Access (CDMA) and so on. In order to spread the bandwidth of the transmitting signals, pseudo-noise (PN) sequences have been used extensively in spread-spectrum communication systems [1]. Obviously, the maximal length shift register sequences (M-sequences) and Gold sequences are the most popular spreading sequences in spread spectrum systems. Many other codes like Walsh code and Chaotic code were reported for the better performance of the CDMA system.

At the receiver end we extract the spreading code in order to retrieve the data from the received noisy signal. This code extraction is done by means of the adaptive channel equalization. Many types of channel equalization techniques like Least Mean Square (LMS), Recursive Least Square (RLS), Decision Feedback Equalizer (DFE) and so on were reported for the code extraction of the CDMA system. All the equalization methods mentioned above are gradient based algorithms. So they suffer from the so called problem in channel equalization local minima. Hence they stick around the local minima and never fall into the global minima. Again the above mentioned equalization techniques are not able to handle the nonlinearity associated with a channel.

To overcome the local minima problem many evolutionary computing methods such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO) and Bacteria Foraging Optimization (BFO) were proposed. As being these techniques are non gradient based algorithm they completely search the search space and fall into the global minima never to the local minima. In this paper we will use GA based channel equalization to improve the performance of the CDMA system.

The section begins with an exposition of the principal motivation behind the work undertaken in this paper. Following this, section III provides a brief literature survey on GA. Section IV outlines the contributions made in this paper. At the end, section V presents the paper layout.

II. DS-CDMA SYSTEM AND OVERVIEW

In this section the principle of spread spectrum and its application in multiple accesses is discussed. Multiple access schemes are used to allow many mobile users to share simultaneously a finite amount of radio channels in a fixed radio spectrum. The sharing of the spectrum is required to achieve high capacity by simultaneously allocating the available bandwidth to multiple users.

A. Spread Spectrum Communication Techniques

As a simple, expansion of the bandwidth is not sufficient to be termed as the spread spectrum, but the bandwidth expansion must be accomplished with the separate signature, known as spreading sequence. Both transmitter and the receiver know this spreading

sequence. It is also independent of the data bits [10]. All the sequences are randomly distributed, and there is no correlation between any two sequences.

B. DS-CDMA Transmitter Principles

The simplest transmitter for downlink of a DS-CDMA is shown in Figure 1. The transmitted signal s(kL + n), at time t = nT_{bit} is constructed by coherently summing the spreading sequence of each user $C_{i,n}$ by those users bit $x_i(k)$ over all active users , to give

$$s(kL+n) = \sum^{U}_{i=1} C_{i,n}\, x_i\,(k) \quad (1)$$

In the uplink case the process is same except that the users are no longer synchronized, and which is modeled by inserting user-specific time delay on the resulting spread

C. DS-CDMA Reciever Principles

The work of the receiver is to recover the data x(n) by converting the spectrum of the received signal vector y□(n). This is done by multiplying the received signal with the required spreading sequence, which is generated locally by the receiver. The received signal, consisting of M_r chips is passed to the block of delay elements, where Z^{-1} represents a delay of one chip, until the complete M_r chip signal has been read. These values are then passed to multiplier block in parallel, which forms the scalar product of y□(n) and the tapweight vector ω_ □C^{Mr} where M_r is the number of tap weights, in this Figure 2 it is 8. This finite impulse response block produces a soft output $\tilde{x}(n)$,which is then passed through the decision block to give a hard estimate, $\tilde{x}(n)$, of the original data bit x(n).

This is the structure of simplest receiver, commonly known as MF receiver with L tap weights w_n: 1≤n≤L matched to the original spreading sequence of the desired user. In practice, synchronization of the chip level signal is a highly non-trivial process. The performance of this receiver has been shown to degrade considerably as the number of simultaneously transmitting users increases. Hence improving the capacity of SS systems is achieved either by reducing the total interference by enhancing the single user detection methods or by making use of multiple access interference (MAI) through improved interference cancellation or multiuser detection technique (MUD).

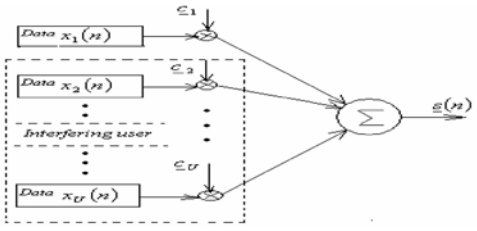


Figure 1. Simplified synchronous DS-CDMA downlink transmitters for U active users.

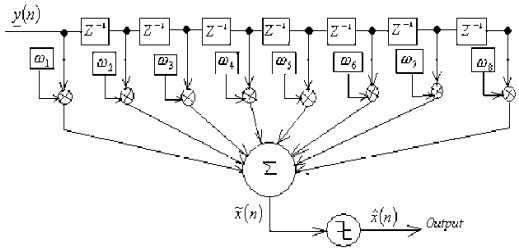


Figure 2. DS-CDMA correlator receiver with 8 tap weights.

D. Pseudo Noise (PN) DS/SS System

Spread spectrum signals for digital communications were originally invented for military communication, but nowadays are used to provide reliable communication in a variety of commercial applications including mobile and wireless communications, which provide resistance to hostile jamming, hide the signal by transmitting it at low power, or make it possible for multiple users to communicate through the same channel. In conventional DS/SS, in order to spread the bandwidth of the transmitting signals, the binary pseudo-noise (PN) sequences have been used extensively in spread spectrum communication (SS) systems. It is a deterministic, periodic signal that is known to both transmitter and receiver, whose appearance has the statistical properties of sampled white noise. It appears, to an unauthorized listener, to be a similar to those of white noise. Therefore, it is not easily intercepted by adversary.

E. Pseudo Noise (PN) DS/SS System

A pseudo random (PN) sequence is a code sequence of 1's and 0's whose autocorrelation has properties similar to those of white noise. Some of the popular PN sequences are Maximal length shift register sequences (m-sequences), gold sequences etc.

E.1 M-Sequence

Maximal length shift register sequences are by definition, thelongest codes that can be generated by a given shift register or a delay element of a given length. In binary shift register sequence generators, the maximum length sequence is 2^n-1 chips, where n is the number of stages in the shift register.

E.2 Gold sequences

For CDMA applications, m-sequences are not optimal. For CDMA, we need to construct a family of spreading sequences, one for each which, in which the codes have well-defined cross-correlation properties. In general, m-sequences do not satisfy the criterion. One popular set of sequences that does are the Gold sequences. Gold sequences are attractive because only simple circuitry is needed to generate a large number of unique codes.

III. INTRODUCTION TO GENETIC ALGORITHM

A pseudo random (PN) sequence is a code sequence of 1's and 0's whose autocorrelation has properties similar to those of white noise. Some of the popular PN sequences are Maximal length shift register sequences (m-sequences), gold sequences etc.

F. Components of Binary Genetic Algorithm

The GA begins, like any other optimization algorithm, by defining the optimization variables, the cost function, and the cost. It ends like other optimization algorithms too, by testing for convergence. In between, however, this algorithm is quite different. A path through the components of the GA is shown as a flowchart in Figure 3.Each block in this "big picture" overview is discussed in detail in this section.

G. Selecting the Variable sand the Cost Function

A cost function generates an output from a set of input variables (a chromo- some). The cost function may be a mathematical function, an experiment, or a game. The object is to modify the output in some desirable fashion by finding the appropriate values for the input variables. We do this without thinking when filling a bathtub with water. The cost is the difference between the desired and actual temperatures of the water. The input variables are how much the hot and cold spigots are turned. In this case the cost function is the experimental result from sticking your hand in the water. So we see that determining an appropriate cost function and deciding which variables to use are intimately related. The term fitness is extensively used to designate the output of the objective function in the GA literature. Fitness implies a maximization problem. Although fitness has a closer association with biology than the term cost, we have adopted the term cost, since most of the optimization literature deals with minimization, hence cost. They are equivalent. The GA begins by defining a chromosome or an array of variable values to be optimized. If the chromosome has Nvar variables (an Nvar-dimensional optimization problem) given by $P_1,P_2,P_3,\ldots,P_{Nvar}$ then the chromosome is written as an N_{var} element row vector.

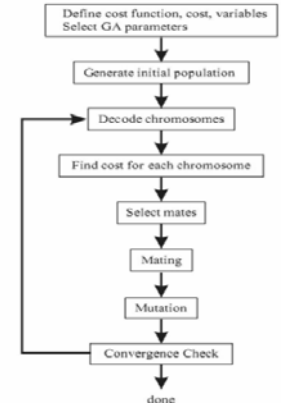


Figure 3. Flowchart of a binary GA.

$$\text{Chromosome} = [P_1,P_2,P_3, \ldots, P_{Nvar}] \quad (2)$$

For instance, searching for the maximum elevation on a topographical map requires a cost function with input variables of longitude (x) and latitude (y)

$$\text{Chromosome} = [x,y] \quad (3)$$

Where Nvar=2. Each chromosome has a cost found by evaluating the cost function, f , at $P_1,P_2,P_3, \ldots, P_{Nvar}$

$$\text{Cost} = f(\text{chromosome}) = f(P_1,P_2,P_3, \ldots, P_{Nvar}) \quad (4)$$

Putative solutions to the target problem are evaluated using "Cost functions", otherwise known as "Objective functions". Based upon the result of such functions, evolutionary pressures may be applied to a set of solutions. The objective function will obviously be problem specific, but there are certain features which should be avoided for the effective application of a GA. Such unfavorable objective functions are discussed below, but often the problems may be alleviated by choosing a different encoding scheme, by normalizing the input parameters, or by rebasing the function. An advantage of GAs over many search or optimization algorithms is that derivatives of this function are not required. This fact ensures that GAs may be readily applied on fitness landscapes (or potential surfaces) which contain discontinuities or singularities without any special treatments [7].

Often the cost function is quite complicated, as in maximizing the gas mileage of a car. The user must decide which variables of the problem are most important. Too many variables bog down the GA. Important variables for optimizing the gas mileage might include size of the car, size of the engine, and weight of the materials.

Other variables, such as paint color and type of headlights, have little or no impact on the car gas mileage and should not be included. Sometimes the correct number and choice of variables comes from experience or trial optimization runs. Other times we have an analytical cost function [8].

H. The Population

The GA starts with a group of chromosomes known as the population. The population has N_{pop} chromosomes and is an N_{pop}-

* N_{pop} matrix filled with random ones and zeros generated using

$$\text{Pop}=\text{round}(\text{rand}((N_{pop},N_{bits}))) \quad (5)$$

Where the function (N_{pop} ,N_{bits}) generates a (N_{pop} , N_{bits}) matrix of uniform random numbers between zero and one. The function round rounds the numbers to the closest integer which in this case is either 0 or 1.Each row in the pop matrix is a chromosome. The chromosomes correspond to discrete values of longitude and latitude. Next the variables are passed to the cost function for evaluation.

I. Selection

Now it's time to play matchmaker. Two chromosomes are selected from the mating pool of

N_{keep} chromosomes to produce two new offspring. Pairing takes place in the mating population until Npop-Nkeep offspring are born to replace the discarded chromosomes. Pairing chromosomes in a GA can be as interesting and varied as pairing in an animal species.

GA selection operators perform the equivalent role to natural selection. The overall effect is to bias the gene set in following generations to those genes which belong to the most fit individuals in the current generation.

There are numerous selection schemes described in the literature; Roulette wheel selection, tournament selection, random selection, stochastic sampling. These, in essence, mimic the processes involved in natural selection.

J. Mutations

The exact purpose of the mutation operations depends upon who you talk to. Mutations enable the GA to maintain diversity whilst also introducing some random search behavior. As for crossover, many types of mutation operator may be conceived depending upon the details of the problem and the chromosomal representation of solutions to that problem.

Random mutations alter a certain percentage of the bits in the list of chromosomes. Mutation is the second way a GA explores a cost surface. It can introduce traits not in the original population and keeps the GA from con- verging too fast before sampling the entire cost surface. A single point mutation changes a 1 to a 0, and visa versa. Mutation points are randomly selected from the Npop * Nbits total number of bits in the population matrix. Increasing the number of mutations increases the algorithm's freedom to search outside the current region of variable space. It also tends to distract the algorithm from converging on a popular solution. Mutations do not occur on the final iteration.

K. The Next Generation

After the mutations take place, the costs associated with the off spring and mutated chromosomes are calculated.

L. Convergence

The number of generations that evolve depends on whether an acceptable solution is reached or a set number of iterations is exceeded. After a while all the chromosomes and associated costs would become the same if It were not for mutations. At this point the algorithm should be stopped [9].

IV. PERFORMANCE OF LINEAR RECEIVERS FOR DS/SS SYSTEM

A direct sequence code division multiple access (DS-CDMA) communications system receiver has three main obstacles to overcome. The first one is multiple access interference (MAI) from other users, which is a direct result of using DS-CDMA. In a cellular system, MAI will be non-stationary due to slow power variations caused by fading and it may undergo step changes when a new user starts or stops transmission (the birth or death of a signal).The transmission channel is responsible for the other two obstacles inter symbol interference caused by multipath and additive noise. To overcome these, many receiver structures have been proposed for the reception of DS-CDMA in a cellular environment.

M. Multi user Receiver

Multiuser receivers [21] are a class of receivers that use knowledge of all the PN sequences to exploit the structure of the MAI. Instead of being separately estimated, as in a single user detection, the users are jointly detected for their mutual benefit. A CDMA receiver can either process the received signal at the chip rate or symbol rate (user bit rate).Figure 4 shows chip rate receivers, which consists of a bank of matched filters (MFs) or RAKEs. A bank of MF sis for the non-dispersive AWGN channel, whereas RAKEs[22] are considered for multipath channels. Current mobiles have a simple RAKE because of its simplicity, whereas base stations can have a bank of MFs (or RAKEs) as depicted in figures 4 and 5. However, structure Figure 4 suffers from MAI and therefore has limited performance. Performance improvement can be gained, when carrier to interference ratio (CIR) information from the interferers is taken into account to combat MAI, as structure in Figure5 suggests. This structure is known as the multi user detector (MUD) and is usually suggested for the asynchronous uplink receiver. It could also be used in a modified version as a single user detector in mobiles and might be implemented in the next generation of mobile systems.

A receiver structure which processes the received signal at the chip rate is known as a chip level based (CLB) receiver. Receivers, shown in Figure 5, which process at the symbol rate and consist of a front end bank of filters, will be called preprocessing based (PPB) receivers.

Because all optimum receivers are too complex for practical applications, the search for simple rand near optimum receivers became vital and goes on. Most proposals are based on the multi user concept, which is preprocessing based (PPB) for several reasons. First, they relate to Verdu's UD receiver, since they consider it optimum.

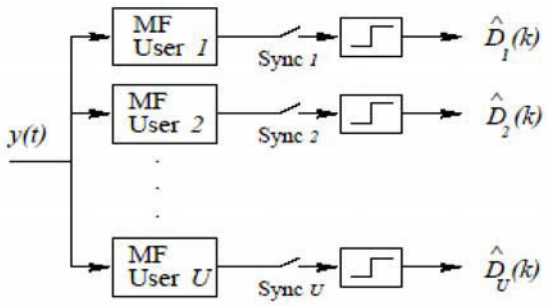


Figure 4. Conventional bank of single user receivers with MFs or RAKEs

N. Matched Filter

The conceptually simplest receiver, the matched filter (MF) receiver, is simply the correlate or receiver with M tap weights, ω_j: $1 \le j \le M$ matched to the complex conjugate time-reverse of the original spreading sequence of the required user which, without loss of generality, we may take to be user 1. The simplest CDMA receiver is the MF receiver, where w is replaced by C_d, the Spreading sequence vector of the desired user. In a multipath fading channel, w corresponds to the convolution between C_d and H_{ch}, implemented as a RAKE.

In practice, the acquisition and synchronization of the chip-level signal is a highly non-trivial task. A very simple and well known detector for SS signals is the matched filter detector, as shown in figure 6. The matched filter detector basically consists of a tapped-delay-line (TDL) filter of which the number of taps equals the spreading sequence length N. The output vector (K) of the tapped delay line

$$\underline{y}(k) = [y(k), y(k-1), \dots, y(k-N+1)]^T \quad (6)$$

is multiplied with a vector of constant weight

$$\underline{w} = [w_0, w_1, \dots, w_{N-1}]^T \quad (7)$$

The resulting scalar product is applied to a decision function e.g. a sign function. For the matched filter case, the weights w_k are matched to the user specific sequence code.

$$w_l = pn_u(N-1-l), 0 \le l < N \quad (8)$$

So that the matched filter output can be summarized as follows:

$$\tilde{D}(k) = \underline{w}^T . \underline{y}(k) = \sum_{l=0}^{N-1} w_l . y(k-l) \quad (9)$$

Provided that the receiver is perfectly synchronized to the transmitter, the TDL extracts a set of chips that represents a particular sequence and the multiplication with the weights is equivalent to dispreading operation. A following decision device such as sign function leads to the final estimate D (k) of the transmitted data bit D(k), hence

$$\hat{D}(k) = sgn\left(\tilde{D}(k)\right) \quad (10)$$

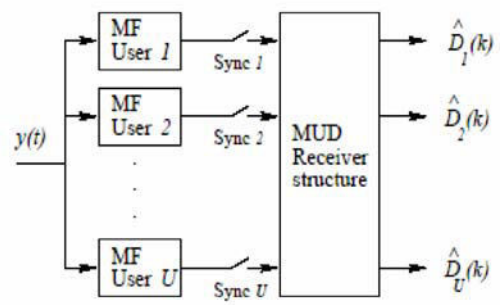


Figure 5. Verdu's proposed multiuser detector scheme with MFs for the AWGN channel

O. MMSE receiver

The motivation for the use of adaptive algorithms lies in the desire to change the individual taps of the receiver filter to respond to changes in the communication channel. The traditional implementation of adaptive receivers is that a sequence of a priori known training data is incorporated into the data stream at prearranged times. It is important to acknowledge that this effectively reduces the overall data rate of the system, which is the main drawback of this approach.

The goal of any adaptive algorithm is to use this training data to force the receiver tap weights to minimize some cost or penalty function, f_{Pen} (.), of the difference metric between the original data bit and its estimated value.

The only requirement for this penalty function is that it be a monotonic increasing function of the absolute value of its argument, with a global minimum at zero. Here, the number of training bits is given by N_{train} and the sequence of training data by $\{x(n): 1 \le n \le N_{train}\}$.

MMSE receiver is an adaptive filter[23] as shown in Figure 7, in which the number of receiver tap weights Nr is set to length of the spreading code M.

The MMSE criteria provide equalizer tap coefficients w(k) to minimize the mean square error at the equalizer output before the decision device. This condition can be represented as

$$j = \varepsilon |e(k)|^2 \quad (11)$$

$$e(k) = s(k-d) - y(k) \quad (12)$$

Where (k) is the error associated with filter output y(k). However, the MMSE criteria optimize the equalizer weights for minimizing the MMSE under noise and ISI. Minimization of MMSE criteria provides equalizers that satisfy the Wiener criterion. The evaluation the equalizer weights with these criteria requires computation of matrix in version and the knowledge of the channel, which in most cases is not available. With this penalty function, the resulting target tap weights have been shown to be given by the Wiener filter, so that these algorithms may be viewed as an iterative approximation to the Wiener filter.

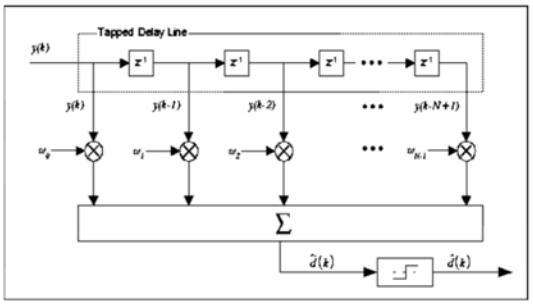


Figure 6. Matched filter.

However, adaptive algorithms like LMS and RLS can be used to recursively update the equalizer weights during the training period.

Two adaptive methods which employ this least square error penalty function are the least mean square (LMS) and the more complex recursive least squares (RLS) algorithms.

LMS algorithm is depicted schematically in Figure 8.

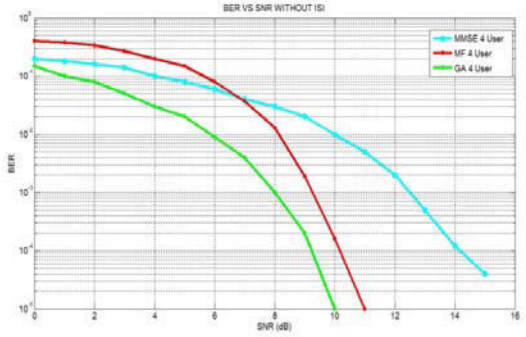
In LMS algorithm, correlation with an FIR filter is performed to obtain a (soft) estimate, x □ , of the training data bit x(n) , as in the correlate or receiver. The error e(n) in this estimate is then used to update the tap weights of the FIR receiver filter. In the LMS algorithm, this is performed by simple weighting of the error by step size u.

V. SIMULATION RESULTS

In order to validate the proposed GA for DS-CDMA applications, extensive simulation studies were conducted. All the simulation studies were conducted on a 2.90GHz Laptop with 4GB of RAM with Microsoft windows seven operating system.

All the simulations are done in Matlab. During the training period the receiver parameters were optimized/ trained with1000 random samples and the parameters so obtained were averaged over 50 experiments. The parameters of the receiver were fixed after the training phase.

Bit error rate (BER) was considered as the performance index. In this section, the BER performance of the different linear receivers like



matched filter and MMSE receiver using gold spreading sequences is done and the performance is compared with GA assisted DSCDMA down link receiver using gold sequences. In all the experiments randomly generated +1/-1samplesweretransmittedforeachuser. In all the simulations, gold sequences of 31chips are considered. These samples were spread using gold sequences of length 31 corresponding to each of the users. For comparison with gold sequences, the maximum permissible **user's in the system is restricted to 31.**

Figure 7. BER performance of different receivers for varying SNR for 4 users being active in the system.

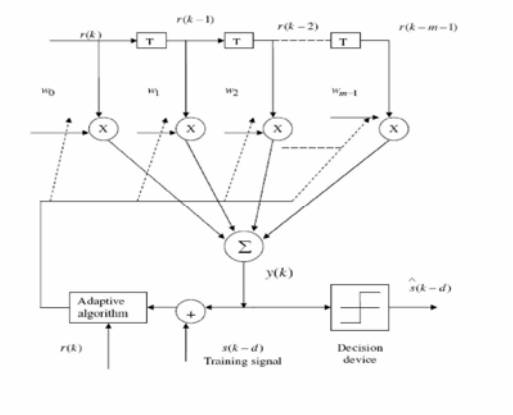


Figure 8. MMSE receiver

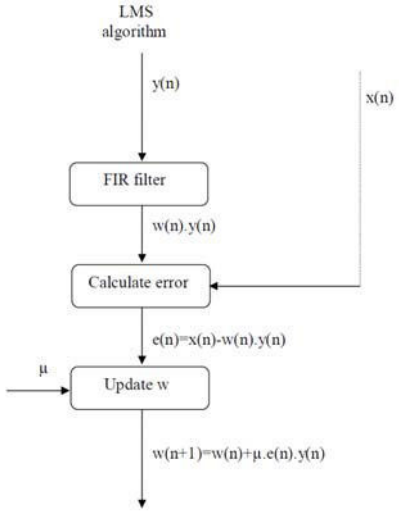


Figure 9. LMS algorithm.

After spreading, the sequences were added and transmitted through the non-dispersive channel. The channel corrupted the transmitted signal with AWGN. The channel output was fed to the various linear receiver structures like Matched filter and MMSE receiver. A total of 10^5 bits were transmitted by each user and a minimum of 1000 errors were recorded. The tests were conducted for different levels of SNR. Additionally tests were also conducted by varying number of active users in the system for fixed value of SNR.

P. Performance comparison of different receivers for channel without ISI.

In Figure 9 performance of different receivers were investigated for varying SNR conditions. Performance gold sequences for 4 users are plotted in Figure 9. It is seen that when the number of users is 4, there is a 1dB performance difference at a BER of 10^{-5} between GA assisted CDMA receiver and the matched filter receiver, and 5dB performance difference between GA assisted CDMA receiver and MMSE receiver.

Q. Performance comparison of different receivers for channel with ISI

In this section, we consider a stationary multipath channel $h=1+0.5Z^{-1}+0.2Z^{-2}$ .In AWGN the number of chips of transmitted is number of chips of the spreading sequence i.e., 31 in this case. In case of multipath channel, inter symbol interference (ISI) is induced from the previous and next symbol into account. So the number of chips will increase. Here, the multipath channel consists of 3 taps. Hence all receiver structures exploit N+ (L-1) = 31+ (3-1) = 33 chips instead of 31. Matched filter is used in AWGN channel whereas Rake receiver is used in Multipath channel.

In Figure 10 performance of different receivers were investigated for varying SNR conditions and the multipath channel $H_{ch}=1+0.5Z^{-1}+0.2Z^{-2}$. In Figure 10 performance of different receivers were investigated for varying SNR conditions. Performance gold sequences for 4 users are plotted in Figure 10.

It is seen that when the number of users is 4, there is a 1dB performance difference at a BER of 10^{-5} between GA assisted CDMA receiver and the matched filter receiver and also for RAKE receiver, and 2 dB performance difference between GA assisted CDMA receiver and MMSE receiver.

CONCLUSION

In this section various linear receivers like Matched filter, MMSE receiver and RAKE receiver is explained. BER performance of different linear receivers using gold sequences is evaluated. It is seen that GA based DS-CDMA receiver performs much better than other type of receivers.

R. Scope of Further Research

Simulations can be extended to some more nonlinear receivers like neural network receivers.

Faster convergence of GA based CDMA receiver can also be investigated.

Simulations can be extended to larger spreading codes like 63,127 chip etc.

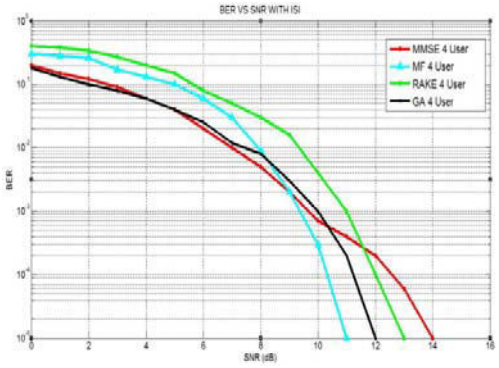


Figure 10. BER performance of different receivers for varying SNR for 4 users being active in the system in multipath channelHch=1+0.5Z^(-1)+0.2Z^(-2).

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NEW CURRENT-MODE MULTIPLIER/DIVIDER

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Abstract— In this paper, a method to reduce the second order effects on the circuit performances caused by the small sized MOS transistors is proposed and a multiplier/divider circuit is designed using this method. The main advantages of the proposed circuit are reduced errors of the output current function, a smaller area on the chip, possibility of controlling the output current with the control voltage, operation at higher frequencies and more efficient power consumption.

Keywords- reducing MOSFET's second order effects; square-root circuit; squarer/divider circuit; multiplier circuit

I. INTRODUCTION

It is well known that the decrease in dimensions of MOS transistor in IC fabrication technology affects MOS transistor performance and the MOS transistor voltage- current relationship changes from square-law to linear. Therefore errors may occur in the output current function of the current-mode circuits employing small sized MOS transistors. In this paper, a method is proposed to reduce the errors generated by the second order effects in the current-mode circuits employing MOS translinear loop, furthermore high-precision multiplier/divider circuit is designed and presented using this method. Analog building blocks such as analog modulator, frequency doubler and etc. can be easily obtained using the proposed multiplier/divider circuit. The output current function of the proposed circuit can be controlled by a control voltage. The proposed method enables the use of much smaller transistors and the circuits to be designed are smaller than their counterparts. Thus they may be operated at much higher frequencies. The proposed circuit is appropriate to be used for filtering in square-root domain, fuzzy logic controllers, artificial neural networks, modulators, phase discriminators, adaptive filters, RMS-DC converters, sine/cosine synthesizers, cryptography systems etc.

II. CURRENT-MODE MULTIPLIER/DIVIDER CIRCUIT

The multiplication of two signals is one of the most important operations in analog signal processing. Recently

several CMOS multipliers have been reported [1-6] and some of them are based on MOS translinear Principle. Translinear circuit principle which was originally formulated for loops of bipolar transistors is generalized and the MOS translinear (MTL) principle is derived by Seevinck [7]. MTL circuits are designed by applying MTL principle and used in synthesizing many nonlinear signal processing functions [8-10]. Square-root circuit and squarer/ divider circuit are two important structures of the MTL circuits. A multiplier/divider circuit can be obtained by using both square-root and squarer/divider circuit as in Figure 1 [11-12].

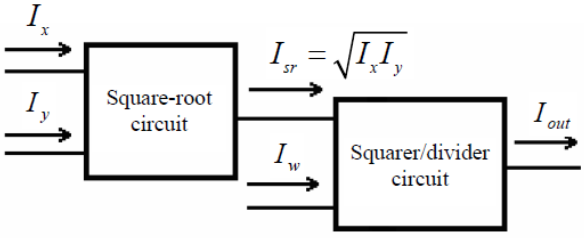


Figure 1. Simplified diagram of the multiplier/divider circuit.

Since Ix and Iy are the input currents of the square-root circuit, the output function of the first circuit can be written as in (1),

$$I_{sr} = \sqrt{I_x I_y} \quad (1)$$

Assuming that this current is the one of the input currents and applying a second Iw to the input, the output current of the whole circuit can be expressed as in (2),

$$I_{out} = \frac{I_m^2}{I_w} = \frac{(\sqrt{I_x I_y})^2}{I_w} = \frac{I_x I_y}{I_w} \quad (2)$$

In order to implement a multiplier/divider circuit, square- root and squarer/divider circuits must be designed. Both square-root circuit and squarer/divider circuit can be obtained by using either the up-down or stacked voltage- trans linear (VTL) loops shown in Figures 1a and 1b, respectively.
Figures 2a and 2b show a possible way of designing the square-root and squarer/divider circuit, using stacked VTL loops [13].
Assume that the aspect ratios of the transistors satisfy the β1=β2=β and β3=β4=2β where β is the transconductance parameter of the MOS transistor, (3) is obtained using theVTL law.

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \quad (3)$$

Assuming that the second order effects are negligable, the drain current of a MOS transistor operated in saturation can be expressed:

$$I_D = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \quad (4)$$

VGS voltage can be obtained from (4) and substituting this term into (3) assuming VTH threshold voltage for each transistor are the same:

$$\sqrt{\frac{2I_1}{\beta}} + \sqrt{\frac{2I_2}{\beta}} = \sqrt{\frac{2I_3}{2\beta}} + \sqrt{\frac{2I_4}{2\beta}} \quad (5)$$

According to Figure 3, the drain currents of M3 and M4 are the same and taking the square on both sides of (5), the equation can be rewritten as:

$$I_3 = \sqrt{I_1 I_2} + \frac{1}{2}(I_1 + I_2) \quad (6)$$

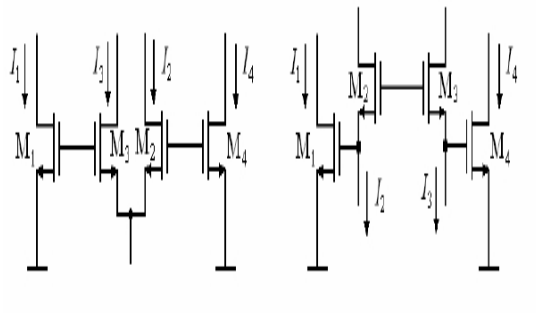
Using the KCL equation at the output node, (7) can be obtained as:

$$I_{out} = I_3 = I_5 - \frac{1}{2}(I_1 + I_2) = \sqrt{I_1 I_2} \quad (7)$$

Equation (7) indicates the function of the current-mode square-root circuit.

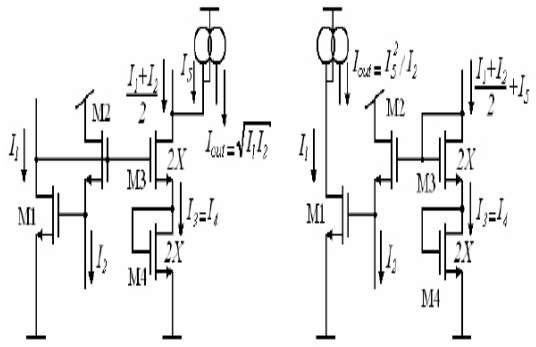
Hence, a square-root circuit can be obtained if I1 and I2 are

the input currents and the output current is a copy of I5. Alternatively, a squarer/divider circuit is obtained if the output is a copy of either I1 or I2 and the inputs are the remaining two currents [14-15].



(a) (b)

Figure 2. (a) Up-down VTL loop. (b) Stacked VTL loop.



(a) (b)

Figure 3. Applications of the stacked VTL loop (a) Square-root cell (b) Squarer/divider cell.

III. PROPOSED CURRENT-MODE MULTIPLIER/DIVIDER CIRCUIT

Nowadays, due to the decrease in dimensions of MOS transistors in IC fabrication technologies, second order effects cause more errors in the MOSFET performance.Actually drain current expression includes effects of W, L and VDS on effective threshold, velocity saturation effects effective mobility dependence on normal field and channel length modulation. Especially, the short-channel effects become more important in MOS transistors at channel lengths of about 1µm or less and require modifications to the MOS models as well as the circuits that are designed using these MOS transistors [16-18]. Due to the second order effects small sized MOS transistors don't operate properly and therefore errors may occur in the output current function of the current-mode circuits employing these transistors. From this point of view, square-root cell and squarer/divider cell which are given in Figure 3 are modified as shown in Figure 4.

The error of the output current function caused by second order effects can be reduced using the resistance R between the gates of the MOS transistors M2, M3 and letting the output current Iout flow through this resistance. In this case, a new voltage term that is added to the VTL loop function which eliminates the error of the output current function. Thus the proposed current-mode multiplier/divider circuit can be realized as shown in Figure 5.

Resistances depicted in Figure 4 are realized with the transistors in Figure 5 and their value can be controlled by the VC control voltages. By this way output current function of the circuit can be controlled and the function errors of the current can be eliminated.

IV. SIMULATION RESULTS

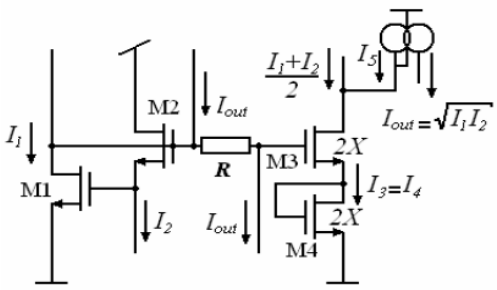
To verify the proposed circuit, SPICE simulations were

performed using TSMC 0.35 µm LEVEL 3 CMOS process parameters. The device dimensions of transistors

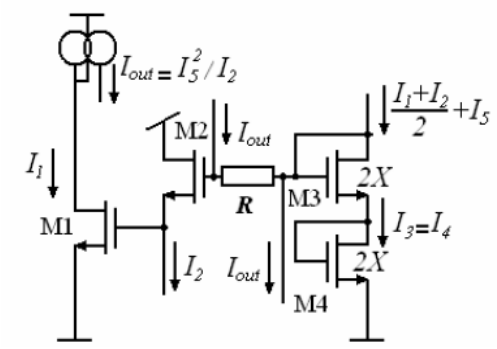
used in the proposed circuit is shown in Table 1. The power supply voltage is 3V.

	W/L [µm]		W/L [µm]		W/L [µm]		W/L [µm]
Ma1	6/.7	**Ma11**	12/.7	**Mb1**	12/.7	**Mb11**	12/.7
Ma2	6/.7	**Ma12**	12/.7	**Mb2**	12/.7	**Mb12**	12/.7
Ma3	12/.7	**Ma13**	12/.7	**Mb3**	24/.7	**Mb13**	12/.7
Ma4	12/.7	**Ma14**	12/.7	**Mb4**	24/.7	**Mb14**	6/.7
Ma5	12/.7	**Ma15**	12/.7	**Mb5**	12/.7	**Mb15**	12/.7
Ma6	12/.7	**Ma16**	12/.7	**Mb6**	12/.7	**Mb16**	12/.7
Ma7	12/.7	**Ma17**	12/.7	**Mb7**	12/.7	**Mb17**	12/.7
Ma8	12/.7	**Ma18**	12/.7	**Mb8**	12/.7	**Mb18**	12/.7
Ma9	6/.7	**Ma19**	10/.7	**Mb9**	12/.7	**Mb19**	80/.7
Ma10	6/.7			**Mb10**	6/.7		

Table 1. Transistor dimensions.



(a)



(b)

Figure 4. Modified current-mode circuits. (a) Square-root cell. (b) Squarer/divider cell.

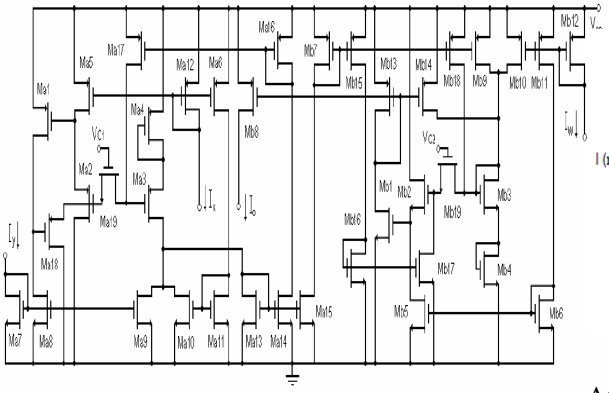


Figure 5. Proposed current-mode multiplier/divider circuit.

To obtain time domain SPICE simulation results of the proposed multiplier/divider circuit, the input current Ix is applied as a triangular wave with an amplitude of 5μA where the other input currents Iy and Iw are constant dc currents with a value of 8μA, as shown in Figure 6. The output currents of the proposed multiplier/divider circuit depicted in Figure 5, the conventional multiplier/divider circuit are observed and simulated with the ideal function as shown in Figure 7. In this simulation VC1 and VC2 are taken 2.09V and 5V respectively.

As expected, the characteristic of the output current function of the proposed multiplier/divider circuit shows approximately the ideal current function and the output current function of the conventional circuit is very different from the ideal curve. The output current function of the proposed circuit can be modified by changing VC1 and VC2 control voltage.

Figure 8 shows the absolute error of the simulated output,
i.e., (IxIy/Iw)-Iz, where the input currents are Ix=Iy= Iw=5(2+sin2πft) μA with f=1MHz.

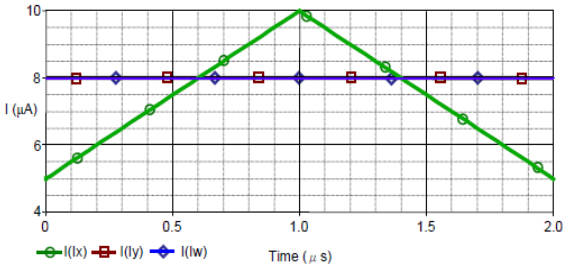


Figure 6. Input currents Ix, Iy and Iw of the proposed multiplier/divider.

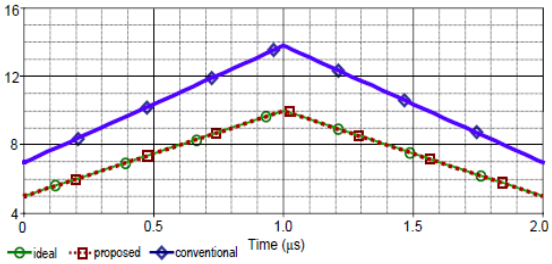


Figure 7. Comparison of the output currents and the ideal curve.

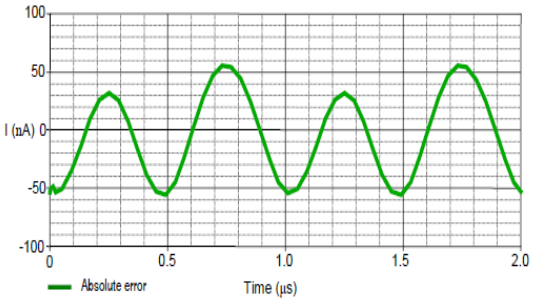


Figure 8. Simulated absolute error of the proposed multiplier/divider.

As shown in Figure 8, the simulated absolute error is less than 0.055μA, thus confirming the high precision of the proposed multiplier/divider circuit. The small-signal bandwidth measured from the input Ix to the output (with Iy=Iw=15μA) is 44MHz as shown in Figure 9.

The DC transfer characteristics of the multiplier/divider circuit are shown in Figure 10. Input currents were Iw=3μA, Iy values ranging from 2μA to 10μA in 2μA steps and Ix swept from 0 to 10μA. As expected, the proposed multiplier/divider circuit shows approximately linear characteristics.

Figure 11 and Figure 12 shows the use of the multiplier as an analog amplitude modulator. Input currents are taken as Ix=5(1+sin2πft) μA with f=0.2MHz, Iy=5(1+sin2πft) μA with f=2MHz and Iw is taken as a fix current of 5μA as shown in Figure 11. The main parameters of the proposed multiplier/divider
circuit are shown in Table 2.

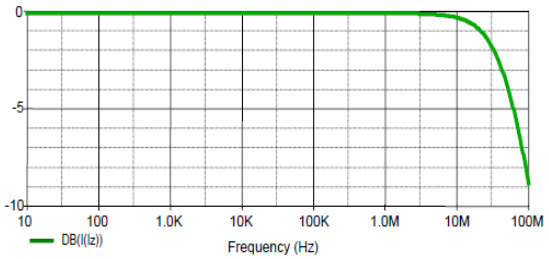


Figure 9. Frequency characteristics of the proposed multiplier/divider.

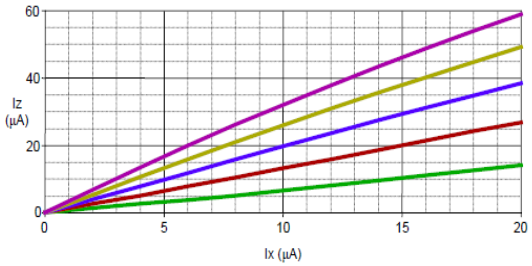


Figure 10. Simulated DC transfer characteristics of the multiplier/divider.

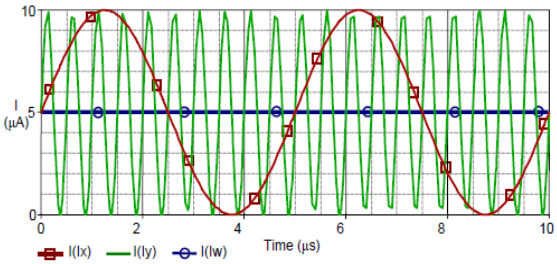


Figure 11. Input currnets of the multiplier/divider as an amplitude modulator.

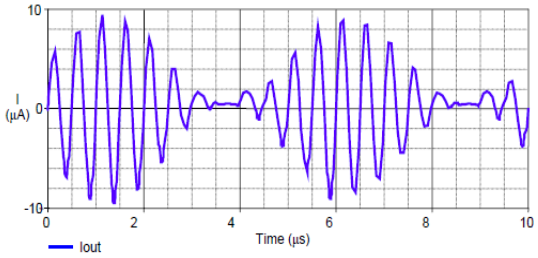


Figure 12. Modulated ac output current of the multiplier/ divider as an amplitude modulator.

Table 2. Performance parameters of the proposed circuit.

Parameter	Value
Technology	0.35 µm CMOS
Supply voltage	3V
THD (input: 10 μA_{pp} at 1 MHz.)	0.144 %
BW (simulated)	44 MHz.
Area	0.01 mm^2
Power consumption (10 µA DC inputs)	0.538 mW

CONCLUSION

In this paper, a method which reduces the errors generated by the second order effects in the current-mode circuits using MOS translinear loop is proposed, also high-precision multiplier/divider circuit is designed using this method. It presents interesting features such as very small area, power efficiency and precision. Hence, it is shown that proposed multiplier/divider circuit is suitable for fuzzy logic controllers, artificial neural networks, modulators, phase discriminators, adaptive filters, cryptography systems, RMS-DC converters, sine/cosine synthesizers etc.

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DESIGNING AN 8 TRANSISTORS 3 TO 2 COMPRESSOR

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Abstract—Compressors are basic components in many applications such as producing partial sums in multiplying. In this paper a new high speed 3 to 2 compressor is presented using 8 transistors and without using a power supply in CMOS logic. Suggested circuit is compared with typical structures to show attained improvements. Mentioned structure insisted on using 3 transistors XOR and PTL 2 transistors multiplexers in building circuits which at last results in high speed and fascinating design. In mentioned structure, despite typical outputs, XOR and multiplexer outputs are used effectively to increase performance and efficiency of the compressors.

Keywords-8 transistors 3 to 2 compressor, high speed, zero statical power consumption

I. INTRODUCTION

In many single goal microprocessors and digital signal processors, multiplying is one of the most important operations in digital processing units which depend on configuring the ALUs and floating point units for performing commands such as convolution and filtering. Basically, multiply consists of 3 steps: first, partial products are produced using an improved encoding to reduce the number of partial products. Then by using compressor circuits which are combined to form Wallace tree, partial products' matrix are reduced to 2 rows. Finally, a 2 input adder is used to add two rows.

As seen clearly, the second phase which is the reduction of partial products has the most critical operation because it is affected by the performance and area of the multiplier. A compressor, in its simplest type, is a circuit which reduces 3 rows of partial products into 2 rows, thus is called 3 to 2 compressor. To increase the speed of compression, several high order compressors, called 7 to 2 and 5 to 2 compressors are presented [2-5].

In many implementations, compressor is located in the critical circuit path, thus request for high speed low power compressors greatly increases [6-8]. This paper presents a new model of 3 to 2 compressor based on using 3 transistors XOR gates. Using these gates causes proper output usage of previous parts and performance improvements of the system. Also rather than these gates, a multiplexer is used to improve time speed in critical path [9].

II. 3 TO 2 COMPRESSORS

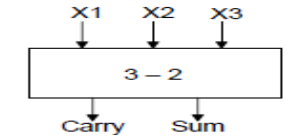
These compressors have 3 inputs X1, X2, X3, two outputs; sum and carry which are shown in Fig.1. Performance equation of 3 to 2 compressor is:

X1+X2+X3=Sum + 2*Carry (1)

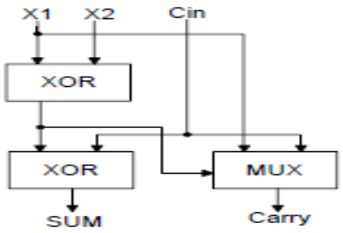
We can use 3 to 2 compressor as a full adder when the third input is a carry bit of previous compressor or when X3=Cin.In Fig 1b we can see traditional implementations of this compressor.this compressor consists of 2 XOR gates ,2 inputs and a 2 to 1 MUX.output equations for this compressor are:

Sum=X1 ⊕ X2 ⊕ X3 (2)

Carry=(X1 ⊕ X2).X3+ $\overline{(X1 \oplus X2)}$,X1 (3)



(a)



(b)

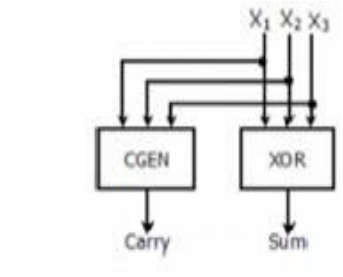
Fig 1(a) .a 3 to 2 compressor (b) Standard implementation of a 3 to 2 compressor.

We can implement this compressor in MCML logic [10]. Diagram and circuit implementations can be seen in Fig 2.

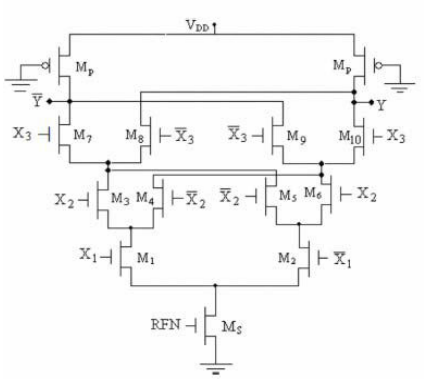
As seen, this circuit consists of one XOR gate and a carry producer unit of CGEN. In this architecture, output equations follow the same initial equations.

As seen, with voltage supply, these circuits need a separate reference voltage. Another defect for this system is the need to 3 inverters for reversing all 3

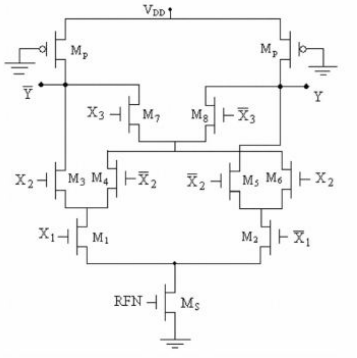
inputs of the compressor which leads to increase in delay and number of transistors and power consumptions.



(a)



(b)



(c)

Fig 2 (a) block diagram of the compressor in MCML (b) MCML(CGEN) carry producing circuit (c) MCML three input XOR/XNOR

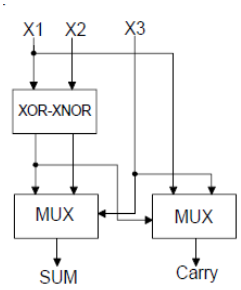
In the third architecture of this compressor, two 2 to 1 MUX and one XOR/XNOR gate are used [11]. Diagram of this architecture and circuit schematics of consisting components can be seen in Fig 3. Equations for outputs of 3 to 2 compressors are:

$$+\overline{(X1 \oplus X2)}.X1 \qquad (4)$$

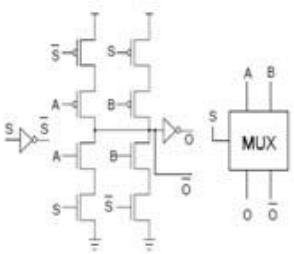
$$Sum=(X1 \oplus X2).\overline{X3}$$

$$Carry=(X1 \oplus X2).X3+\overline{(X1 \oplus X2)}.X1 \qquad (5)$$

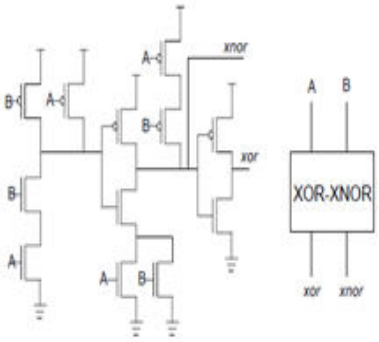
As seen, carry Equations are the same in first and third architecture and the difference between these two is only in sum equations. This circuit has better performance than traditional implementations.



(a)



(b)



(c)

Fig 3 (a) third architecture block diagram (b) MUX circuit (c) XOR/XNOR gate circuit in third architecture

III. SUGGESTED CIRCUIT

Our main goal is building a 3 to 2 compressor by the least number of transistors in CMOS logic. The clear thing is that compressor components often consist of MUX and XOR gate. As observed, we need to use a XOR gate in a 3 to 2 compressor. To implement of presented gate in Fig 3c we need 12 transistors, so this causes increase in power consumption and occupied area on a silicon surface, thus this is not a proper circuit. By introducing PTL circuits a new approach was presented for electronic circuits and VLSI. In such circuits there was no power supply, thus static power reduced. On the other hand, by reducing the number of transistors, essential surface for implementations also decreases.

In figure 4 the circuit schematic of a 3 transistors XOR gate can be seen [12]. This circuit has no static power and occupies little area.

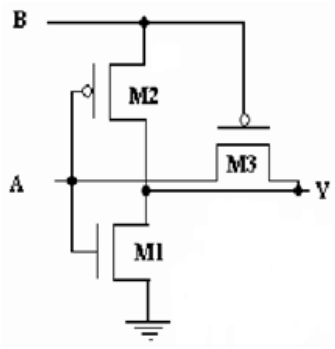


Fig 4. 3 transistors XOR gate implementation.

By using this gate, in the architecture type 1, we can have the least number of transistors (18 transistors).

It's notable that in a 12 transistors XOR gate, first, XNOR output is produced and then main output is produced by using an inverter. This causes increase in power consumption. This is also true for MUX, so that the final response is achieved by passing an inverter. Pay attention that the number of all unused outputs is decreased using outputs and their complement and finally the total power consumption and required number of transistors [13-15]. So our suggested compressor follows first architecture and consists of two 3 transistors XOR, and one PTL 2 transistors MUX, as seen in Fig 5.

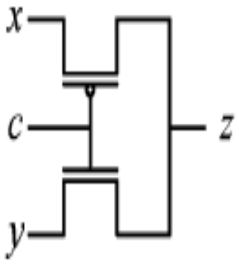


Fig 5. 2 transistors mux gate implementation

IV. SIMULATION AND RESULT ANALYSIS

Circuit simulation was done using HSPICE software with 180nm technology in the range of 0.9 to 3.3V and all the inputs were supplied by 100 MHz frequency.

In tables 1, results of new circuit and previous implemented samples in CMOS logic in voltages of 1.2 to 3.3 V are given.

The results indicate that output delay of new compressor is constant and in compared to the least time delay of suggested reference circuits [11], [16] are improved by 99.97% and 99.98% respectively.

In fig. 6 we can see input pulses with different delays, so that conditions for different inputs are created.

Table 1. comparing delay of suggested circuit and existing circuits in respect to nS for 3 to 2 compressor

	1.2	1.8	2.5	3.3
[11]	1.87	1.36	1.21	0.82
[16]	7.59	2.45	1.43	1.05
Suggested Circuit	0.0002	0.0002	0.0002	0.0002

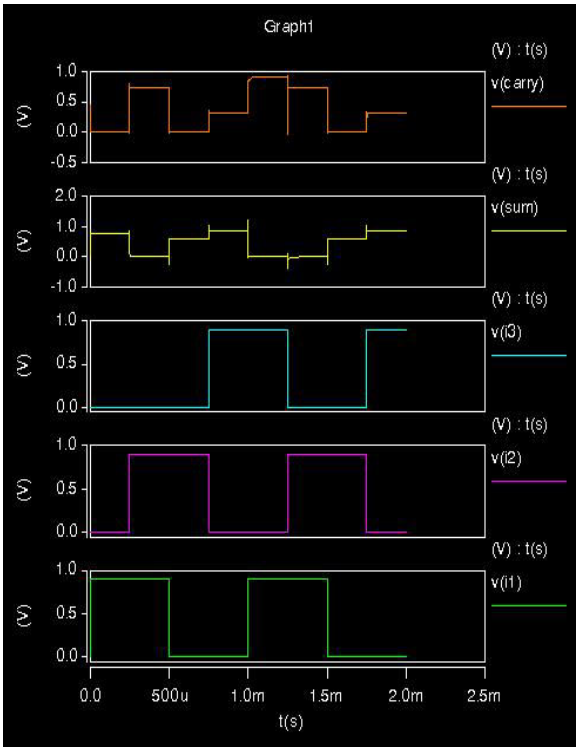


Fig 6. input and output diagram of 3 to 2 compressor .

CONCLUSION

In this paper we have proposed a new 3 to 2 compressor in CMOS logic using 8 transistors. New compressor has no static power consumption because of using no power supply. This compressor has a delay of 0.0002 ns.

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